NEUROPIXELS 2.0

User Manual

February 9, 2024

Important Information

THE NEUROPIXELS PROBES **ARE ONLY INTENDED FOR RESEARCH USE ONLY ("RUO") IN NON-HUMAN SUBJECTS** SUCH AS SMALL ANIMALS INCLUDING RODENTS AND NON-HUMAN PRIMATES. THESE NEUROPIXELS PROBES **SHOULD NOT BE USED IN HUMANS AND ARE NOT MANUFACTURED OR APPROVED FOR HUMAN USE**. THEY HAVE **NO PROVEN HUMAN EFFICACY AND ARE NOT INDICATED FOR HUMAN USE OR ANY FORM OF CLINICAL USE**.

About Neuropixels

The Neuropixels 2.0 neural probe is an advanced silicon CMOS digital integrated microsystem and a tool for neuroscience research. It was developed through a collaboration funded by Howard Hughes Medical Institute (HHMI), University college London (UCL), The Flemish Institute for Biotechnology (VIB), the Catholic University of Leuven (KUL), The Norwegian University for Science and Technology (NTNU, and the Champalimaud Centre for the Unknown. Probes were designed, developed and fabricated at imec, Leuven, Belgium in collaboration with Howard Hughes Medical Institute (HHMI), University college London (UCL), The Flemish Institute for Biotechnology (VIB), the Catholic University of Leuven (KUL), The Norwegian University for Science and Technology (NTNU), and the Champalimaud Centre for the Unknown.

Legal Disclaimer

List of abbreviations

AP	Action Potential.
API	Application Programming Interface.
ASIC	Application Specific Integrated Circuit.
BIST	Built-In Self-Test.
CMOS	Complementary Metal-Oxide-Semiconductor.
DIW	De-Ionized Water.
EEPROM	Electrically Erasable Programmable Read-Only Memory.
ESD	Electro-Static Discharge.
FPC	Flexible Printed Circuit.
FPGA	Field Programmable Gate Array.
GND	Ground.
HS	Headstage.
HST	Headstage Test Dongle.
ID	Identification.
I/O	Input and/or Output.
IPA	Isopropyl Alcohol.
LDO	Low-DropOut.
LED	Light-Emitting Diode.
LFP	Local Field Potential.
MSVC	Microsoft Visual C++.
MXI	Multisystem eXtension Interface.
NI	National Instruments.
PBS	Phosphate-Buffered Saline.
PCB	Printed Circuit Board.
PC	Personal Computer.
PCIe	Peripheral Component Interconnect Express.
PXIe	PCI eXtensions for Instrumentation express.
REF	(External) Reference.
RT	Room Temperature.
SEM	Scanning Electron Microscope.
SMA	Sub-Miniature version A.
SMD	Surface-Mount Devices.
USB-C	Universal Serial Bus Type-C.
ZIF	Zero Insertion Force.

Definitions of technical terms

- ASIC: Integrated circuit that contains recording electrodes, amplifiers, multiplexers and digitizers.
- Probe Shank: Implanted part of the probe ASIC.
- Probe Base: Non-implanted part of the probe ASIC.
- Flex: Flexible PCB (or FPC) onto which the probe ASIC and additional passive and active components are mounted. It connects to the HS.
- Control System: System components required to enable control of and data streaming from Neuropixels probes. These entail the headstage, interface cable and PXIe acquisition module or OneBox.
- Headstage: Miniature board that enables reliable power supply to the probe and is essential for bi-directional data communication from/to the probe (Figure 10).
- Headstage Test Dongle: a small test box that plugs into the ZIF connector of a headstage. Its purpose is to help verify the functionality of a headstage.
- Interface Cable: Thin and flexible cable for power and bidirectional data transmission between HS and PXIe acquisition module or OneBox (Figure 12).
- PXIe Acquisition Module: Custom-made PCB module with two FPGAs for probe configuration, data acquisition and transmission to PC via PCIe interface (Figure 13).
- Port: USB-C plug on the front panel of the PXIe acquisition module or OneBox. The PXIe acquisition module front panel contains 4 ports (Figure 13) allowing connection of up to 4 interface cables. The OneBox front panel contains 2 ports.
- PXIe Chassis: Houses PXIe modules and connects them with a high-performance backplane that offers timing and synchronization capabilities.
- Driver: The software files that need to be installed on the host PC to enable communication with the Neuropixels control system and to develop custom application software.
- Dock: The headstage connects to the probe, using a ZIF connector. Each ZIF connector is referred to as dock.

Table of Contents

1 About This Manual

This document describes the key features of the Neuropixels 2.0 probe and control system and how to install them prior to use. The Neuropixels hardware consists of:

- The Neuropixels probe.
- The Neuropixels control system which contains:
  - A headstage.
  - An interface cable.
  - A PXIe acquisition module or OneBox (coming soon)
- A headstage test dongle (coming soon)

Even if you have read articles on the Neuropixels 2.0 probes and feel that you are familiar with using the Neuropixels probes we request and encourage you to carefully read the latest version of this *User Manual* to refresh your knowledge and remain up to date on possible changes that are relevant to the use of your probes.

If you are unfamiliar with the Neuropixels probes, then it is absolutely essential and imperative that you carefully read the complete *User Manual*.

Please check www.neuropixels.org for the latest version of this manual.

1.1 Related Documentation

The following documents and online resources contain information that you might find helpful as you read this manual:

- Wiki: https://github.com/cortex-lab/neuropixels/wiki.
- Application Software:
  - SpikeGLX: http://billkarsh.github.io/SpikeGLX/.
  - Open Ephys: https://open-ephys.github.io/gui-docs/User-Manual/Plugins/Neuropixels-PXI.html .
- Brochures and technical datasheets:
  - Neuropixels 2.0 Probe (available on www.neuropixels.org).
  - Control System (available on www.neuropixels.org).
- Mechanical drawing of the aluminum metal cap (available on www.neuropixels.org).

2 Getting Started

2.1 Unpacking and Handling

Upon receiving the Neuropixels probe and control system, immediately inspect the shipping boxes and content for damage. In case of damage, please carefully read the included warranty document and follow the instructions.

The probes arrive in black shipping boxes containing black foam inlays. Both the box and foam inlays are manufactured from ESD compliant (antistatic) material. All system components are also delivered in antistatic bags or boxes. It is advised to wear ESD protective equipment when handling the probes and system components. Carefully read the guidelines on probe handling (**Appendix A**), soldering (**Appendix B**) and ESD safety (**Appendix C**).

2.2 Hardware & System Requirements

2.2.1 PXIe acquisition module control system

Figure 1 shows the Neuropixels 2.0 probe and the PXIe acquisition module control system that can be purchased from imec through www.neuropixels.org. To get started you need:

- one PXIe acquisition module (PXIE_1000),
- one data/power interface cable (CBL_1000),
- one headstage (HS_2010) and
- at least one probe.

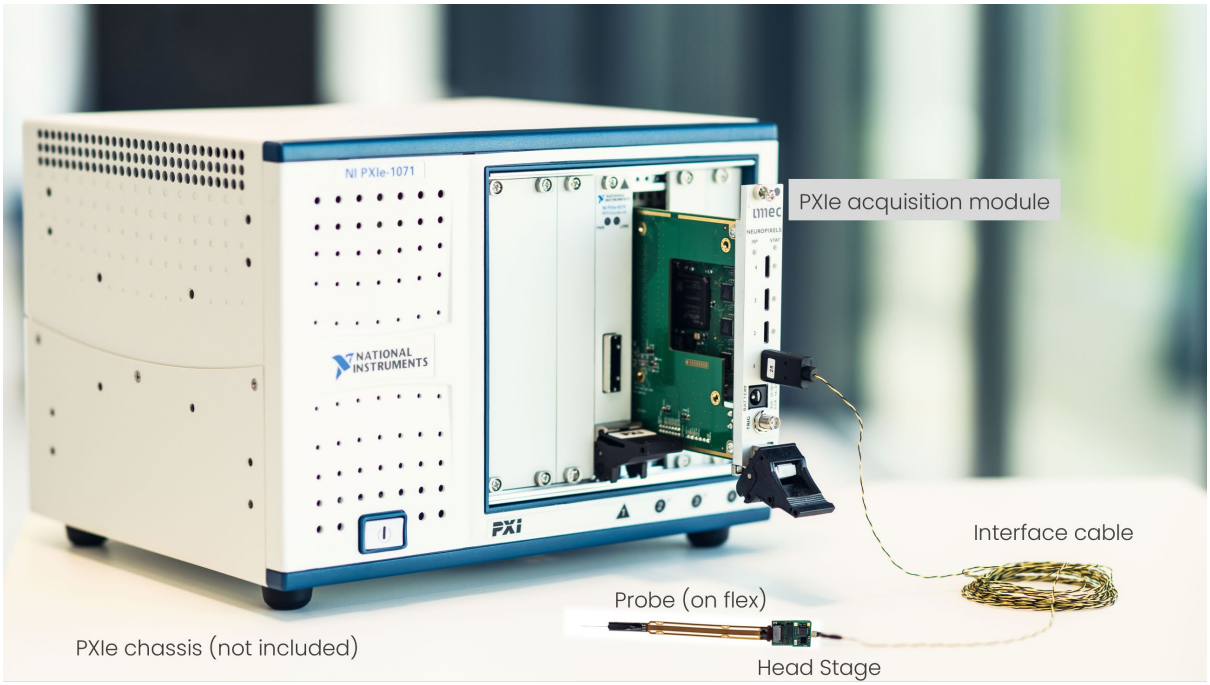


Figure 1: Neuropixels 2.0 probe and control system (chassis not included)

In addition, the PXIe chassis required for using the PXIe acquisition module must be purchased separately from third-party suppliers such as National Instruments (NI)[1], Keysight[2] or Adlink[3]. Below we provide recommendations for PXIe chassis using a remote controller (MXI-Express interface) and a PXIe chassis with built-in Thunderbolt 3 remote controller (link). A detailed description of the system requirements can be consulted on the SpikeGLX website.

For first-time probe users intending to use less than 3 PXIe acquisition modules simultaneously, we recommend the following entry-level chassis with build in Thunderbolt card:

- PXI-Express chassis: NI PXIe-1083 (5-Slot). PN 787026-01
- Power cord for chassis.
- Thunderbolt 3 Type-C Cable, Passive 20 Gbps, 5A, 2m. PN 785608-02

For more advanced, multi-probe users planning to use multiple PXIe acquisition modules simultaneously, we recommend the system with the highest bandwidth:

- PXI-Express chassis: NI PXIe-1088. PN 784782-01
- Power cord for chassis.
- MXI-Express interface: NI PCIe-8389 and PXIe-8389 (Gen 3 x16, 1 Port; incl. one MXI-Express x16 copper cable, 3m). PN 784177-01

Other chassis-remote controller combinations are technically possible. A list of combinations is given in Table 1 below:

[1] https://ohm.ni.com/advisors/pxi/pages/common/intro.xhtml
[2] https://www.keysight.com/us/en/home.html
[3] https://www.adlinktech.com/en/index

Table 1: Data acquisition configurations

Config	PXI-chassis		Remote controller		Data Acquisition		Bandwidth
	Name	PN	Name	PN	Name	PN	
Thunderbolt	NI PXIe-1083	787026-01	-	-	Imec card	PXIe_1000	2 GB/s
Thunderbolt (Figure 2)	NI PXIe-1071	781368-01	PXIe-8301	785679-01	Imec card	PXIe_1000	2.3 GB/s
PXIe-PCIe	NI PXIe-1088	784782-01	PXIe-PCIe 8398	784177-01	Imec card	PXIe_1000	16 GB/s
PXIe-PCIe	NI PXIe-1082	End of Life	PXIe-PCIe 8398	784177-01	Imec card	PXIe_1000	16 GB/s
PXIe-PCIe (Figure 3)	NI PXIe-1082	End of Life	PXIe-PCIe 8381	End of life	Imec card	PXIe_1000	2.3 GB/s
PXIe-PCIe	NI PXIe-1071	781368-01	PXIe-PCIe 8381	End of life	Imec card	PXIe_1000	2.3 GB/s
OneBox	-	-	-	-	-	ONE_1000	USB 3.0

Figure 2: PXIe chassis PXIe-1071 & Thunderbolt PXIe-8301

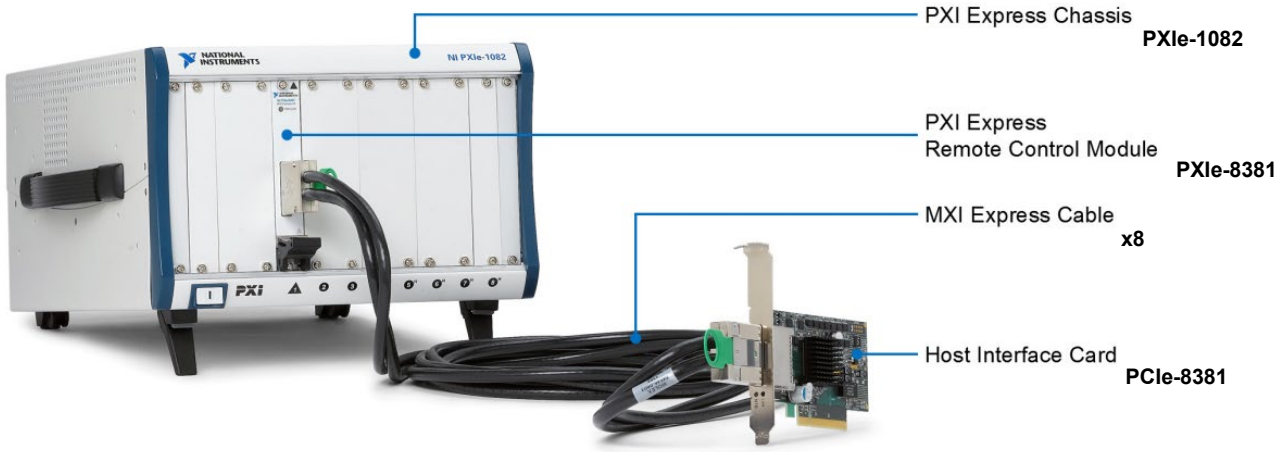


Figure 3: PXIe-8381 (remote control module) and PCIe-8381 (host interface card) allow desktop PC control of a PXI Express chassis with PCI Express Gen 2 x8 data throughput.

A host PC is needed for recording the neuronal data. Make sure the following PC specifications are fulfilled:

- PC Administrator rights.
- Windows 10.
- Dedicated solid state drive for data streaming.
- Intel motherboard
- In case you are using a thunderbolt configuration, make sure a thunderbolt 3 port is available on the host PC. In case of a PXIe-PCIe interface, make sure at least one PCIe slot (Gen 2 x8 or wider) is available to install the PXIe remote controller.

Please refer to the OpenEphys or SpikeGLX website for exhaustive PC requirements.

Chapter 4 in this *User Manual* contains further instructions on how to install the above hardware.

***NOTE**: If you decide to use the existing application software packages SpikeGLX or Open Ephys described in **Section 2.4.1**, please consult the respective software User Manual and/or online Documentation to ensure you also comply with these system requirements.*

2.2.2 OneBox control system

Coming soon

2.3 Drivers

2.3.1 PXIe acquisition module control system

To install the Neuropixels PXIe acquisition module you need to download the following PXIe Acquisition Module driver files from the SpikeGLX GitHub site.

- *EnPcieDriverWin.inf*
- *EnPcieDriverWin.sys*
- *WdfCoInstaller01009.dll*
- *enpciedriverwin.cat*
- *Version_1.9_readme.txt*

Section 4.1.3.2 of this *User Manual* describes how to install the driver.

2.3.2 OneBox control system

Coming soon

2.4 Application Software

2.4.1 Existing Software

You can acquire data from Neuropixels 2.0 probes with either of two existing software packages: SpikeGLX[4] or Open Ephys[5]. The former is being developed by Bill Karsh at Janelia Research Campus. The Open Ephys GUI is a plugin-based application for extracellular electrophysiology data acquisition and is being developed by Josh Siegle and Jakob Voigts.

Both packages use the same underlying Neuropixels API to communicate with the probes, so their functionality as far as acquiring data should be identical, though they differ in their online graphical display, interface for modifying probe settings, options for online data processing, and file formats for saving data.

SpikeGLX is distributed with an extensive *User Manual* while Open Ephys has a detailed online *User Documentation* section. To install the software and configure the probes, carefully read these documents and follow the instructions.

***NOTE**: Each of the above software packages may require additional third-party hardware or software installations. Please read the respective software User Manual or online Documentation to ensure you meet all PC and system requirements.*

[4] http://billkarsh.github.io/SpikeGLX/
[5] https://open-ephys.github.io/gui-docs/User-Manual/Plugins/Neuropixels-PXI.html

2.4.2 Developing New Software

If you are interested to develop your own application software, you will need the 32-bit or 64-bit windows *.dll, .lib*, and *.h* files for the API driver. These files and the complementary *API Manual* are available upon request. The API is compatible with MSVC and MinGW.

2.5 Probe Configuration File

The probe-specific configuration file will be provided with each probe shipment via the WeTransfer file transfer service to the technical contact person listed on the sales order. The provided configuration file must be loaded into the software prior to using the probes. This file is essential to correct for CMOS processing-induced deviations of probe performance.

Details on how to load this file into the application software are described in the respective *User Manual* and *User Documentation* of SpikeGLX and Open Ephys.

In case you lost the calibration files of your probes or in case the WeTransfer link expired, please contact neuropixels.sales@imec.be . They will provide you with the correct calibration files.

3 Neuropixels Hardware Description

3.1 Probe

The Neuropixels 2.0 multi shank probe is a silicon CMOS digital integrated microsystem and tool for in vivo neuroscience research in small animals. The probe features 5120 low-impedance TiN recording sites densely tiled along four thin, 10 mm-long, straight shanks, which have a pitch of 250 µm. The 384 parallel, configurable, low-noise recording channels integrated in the base enable simultaneous, full-band recording of hundreds of neurons. The electrodes are arranged in a linear double row layout. Additional specifications are provided in Table 2, Table 3 and *Table 4*.

Table 2: Electrode specifications

ELECTRODES	
NUMBER	5120
PATTERN	Linear, two rows
PITCH	15 µm (column), 32 µm (row) (see Figure 4)
MATERIAL	Porous TiN
SIZE	12 × 12 µm
IMPEDANCE	~150 kΩ (at 1 kHz in PBS)
SELECTIVITY	Local switch under each electrode

Table 3: Shank specifications

SHANK PROPERTIES AND MATERIALS	
NUMBER	4
SHANK PITCH	250 µm
WIDTH	70 µm
LENGTH	10 mm
THICKNESS	24 µm
BENDING	≤200 µm (base to tip)
TIP LENGTH	175 µm
TIP SHAPE	Chisel
TIP ANGLE	~20°
FRONTSIDE MATERIAL	Silicon nitride (Si_3N_4)
BACKSIDE MATERIAL	Silicon dioxide (SiO_2)
SIDEWALL MATERIALS	Silicon (Si), silicon dioxide (SiO_2)

Table 4: Recording channel specifications

RECORDING CHANNELS AND DIGITAL INTERFACE	
NUMBER	384 (full-band)
BANDWIDTH	0.5 Hz - 10 kHz
AP INPUT-REFERRED NOISE	~6.8 μV_{rms} (typical[6])
LFP INPUT-REFERRED NOISE	~5 μV_{rms} (typical)
AP SAMPLING FREQUENCY	30 kHz
GAIN	100
CROSSTALK	1.51% (at 1 kHz; typical)
INPUT VOLTAGE RANGE	10 mV_{pp}
ADC RESOLUTION	12 bits
DATA RATE	144 Mb/s
POWER CONSUMPTION	~22 mW (in recording mode; typical)
SHANK HEATING	<1°C (in the brain)

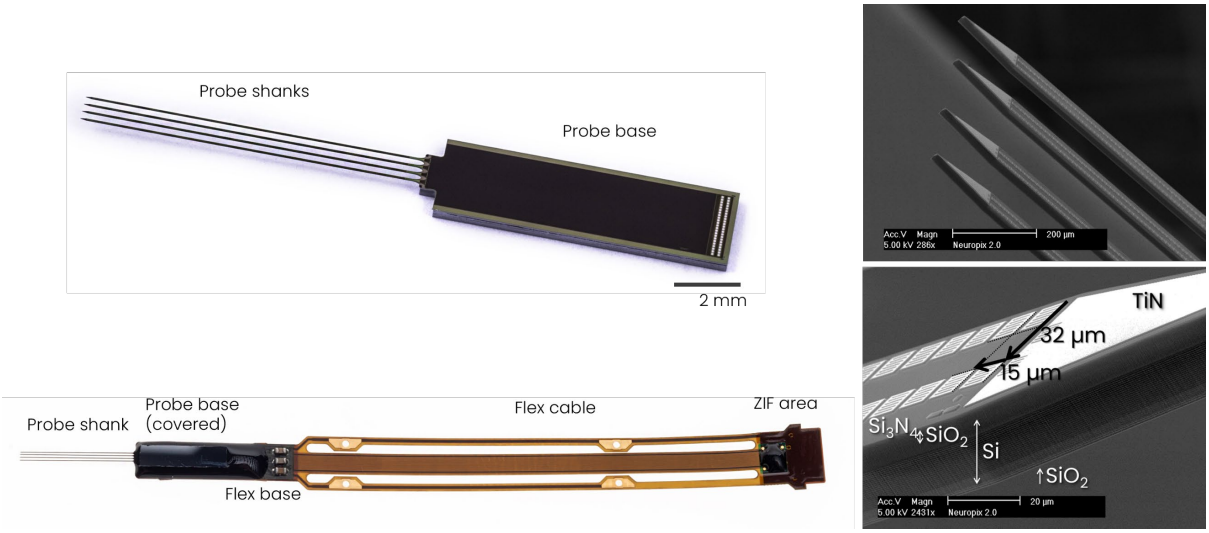


Figure 4: Top left: Bare die of the Neuropixels 2.0 multishank probe ASIC. Bottom left: Packaged probe ASIC with silicon spacer covering the probe base. The SMD components are covered with conformal coating. Right: SEM images of the probe tip with marked electrode pitch and exposed materials.

The probe ASIC is packaged (glued and wire-bonded) on a flexible polyimide printed circuit board populated with several SMD components (Figure 4). The components include passives for biasing and decoupling, and an EEPROM for probe identification. There are multiple input pads for external reference (REF) and ground (GND) along the narrow side arms of the flex cable (Figure 5). These side arms can be cut to length or completely removed when not used.

***NOTE**: Please be careful when cutting the narrow side arms of the flex. Use a pair of fine, pointed scissors. Avoid any damage to the wider middle section of the flex since this can render the probe non-functional.*

[6] Process corner

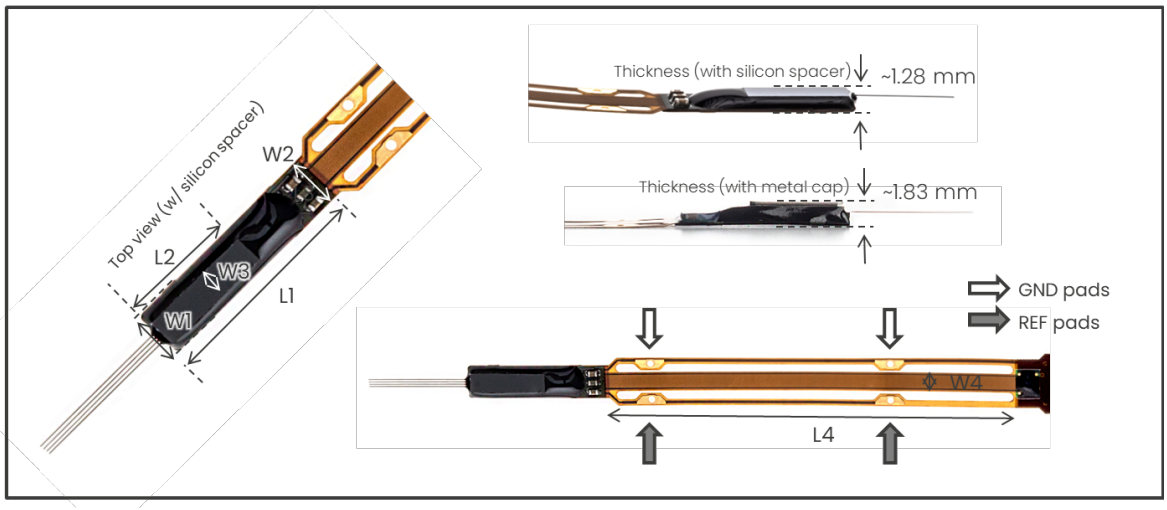


Figure 5: Left: Dimensions of a probe package with silicon spacer. Top right: Thicknesses of the probe package with silicon spacer and probe package with metal cap. Bottom right: Dimensions of the flex and locations of REF/GND pads along the flex. Dimensions are in mm.

Each probe has a unique identifier code stored on the EEPROM and written on the small label attached to the ZIF area (Figure 6). The acquisition software packages described in Section 2.4.1 automatically read the probe ID stored on the EEPROM.

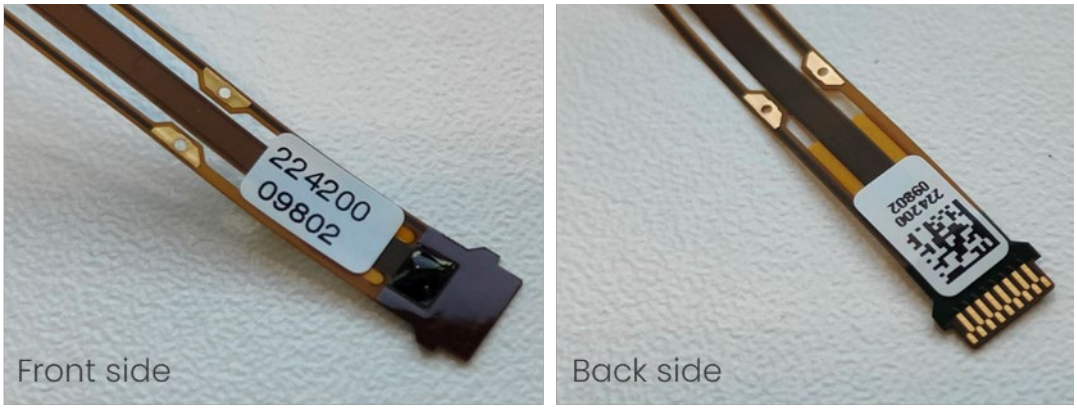


Figure 6: Left: Label with unique probe ID attached to ZIF area front side. Black epoxy covers the EEPROM. Right: ZIF area back side with metal contact pads and unique probe ID and QR code.

The probe base is covered either with a 300-µm-thick silicon spacer (7.8 × 2 mm) or aluminum metal cap (8.0 × 1.8 mm) with dedicated dovetail structures (Figure 9). Each probe cover serves primarily as a light shield for the light-sensitive circuits in the probe base but also enables alignment and attachment of compatible stereotactic insertion drives developed amongst others at HHMI Janelia Research Campus. The HHMI design is manufactured at imec and can be purchased via the RFQ form under the order code HOLDER_2000_C. The holder is shown in Figure 7 and Figure 8 below.

Figure 7: Neuropixels 2.0 probe with Cap and the dove tail holder (HOLDER_2000_C)

Figure 8: Neuropixels 2.0 probe mounted on the dedicated dove tail holder (HOLDER_2000_C)

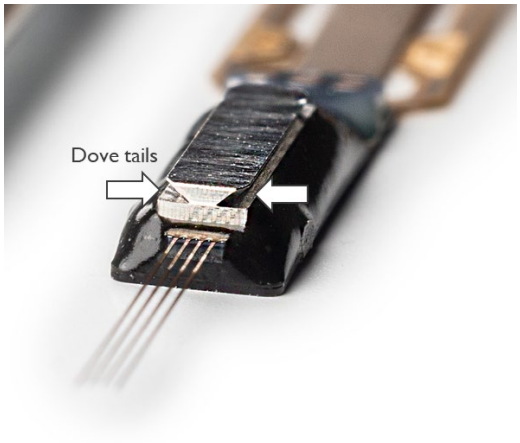


Figure 9: Probes with aluminum cap featuring dedicated dovetail structures.

A black epoxy (EPO-TEK/H70E) encapsulates the probe perimeter and bond wires. The SMD components are also coated with a conformal, hermetic coating (ELPEGUARD/SL 1307 FLZ-T). The probe package with silicon spacer weighs 163 mg and the one with a metal cap 183 mg. The respective thicknesses at the probe base are ~1.28 mm and ~1.83 mm for the two packages (Figure 5). Table 5 summarizes the package dimensions and properties.

Table 5: Probe package description

PACKAGE DESCRIPTION	
WIDTH AT PROBE BASE	3.5 mm
WIDTH AT SMD BASE	3.5 mm
WIDTH OF SILICON SPACER	2.0 mm
WIDTH OF METAL CAP	1.8 mm
WIDTH OF FLEX	2.0 mm
LENGTH OF PROBE + BASE SMD	14 mm
LENGTH OF SILICON SPACER	7.8 mm
LENGTH OF METAL CAP	8.0 mm
LENGTH OF FLEX	42 mm
THICKNESS AT PROBE BASE	~1.28 mm (with Si spacer) ~1.83 mm (with metal cap)
THICKNESS OF FLEX	80 µm
EXTERNAL REFERENCE INPUT	REF (multiple pads along flex)
GROUND INPUT	GND (multiple pads along flex)
BLACK EPOXY	EPO-TEK / H70E
CONFORMAL COATING OF SMD	ELPEGUARD / SL 1307 FLZ-T
WEIGHT	~183 mg (with Si spacer) ~183 mg (with metal cap)

***NOTE**: Please carefully read and follow the guidelines on soldering (Appendix B) before soldering separate wires to the REF and GND input pads. It is advisable to have prior experience in soldering before soldering to the Neuropixels probes.*

***NOTE**: Please carefully read and follow the instructions on probe handling (**Appendix A**) and ESD protection (**Appendix C**) prior to handling any Neuropixels system components. Familiarize yourself with the probes by first handling and testing dummy probes which can be ordered separately.*

3.2 Headstage

The HS (Figure 10) is 10 x 14 mm and weighs 0.7 g. It contains several LDO regulators for power supply, a serializer chip for communication to/from the PXIe acquisition module or OneBox, and an EEPROM for identification. The headstage contains 2 * 17-pin ZIF connectors (docks), to plug in two probes (Figure 10). The docks are numbered 1 and 2, which is visible in copper layer on the PCB, and are located on the front and back side of the headstage. A 4-pin Omnetics connector plugs into the 5-m long twisted-pair interface cable (Figure 12).

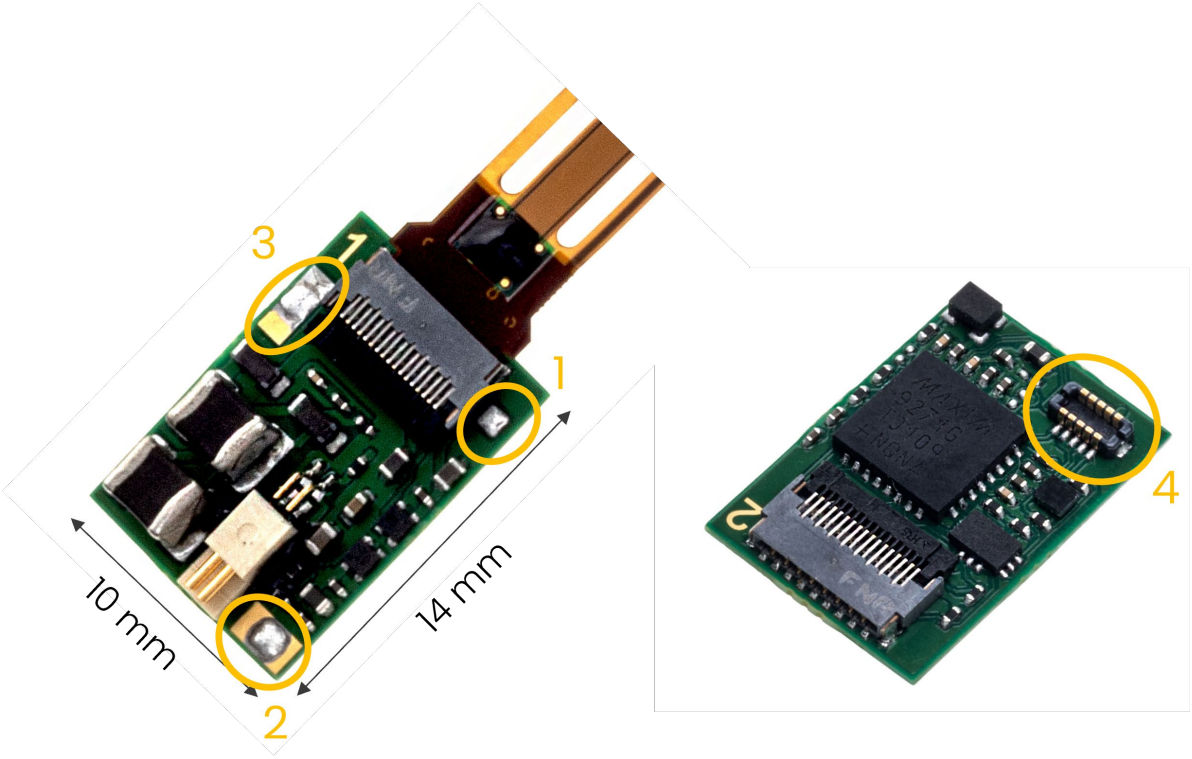


Figure 10: Left: Front side of a headstage with ZIF connector (dock 1) plugged to a probe and Omnetics connector to the interface cable. Location of the solder pads are indicated in orange (1=CAL_SIGNAL, 2=GND, 3=LESION): Right: Back side of the headstage with ZIF connector to probe 2 (dock 2). Location of the extension board connector is indicated in orange (4=extension board connector).

There are three solder pads (GND, LESION and CAL_SIGNAL) on the headstage, as indicated in Figure 10 left. The CAL_SIGNAL is intended only for internal imec use. Extension wires can be soldered to these pads. Follow proper ESD and soldering guidelines.

An extension board connector (Figure 10 right) is added to the headstage which gives access to the I2C bus of the serializer component on the headstage. The board-to-board connector is model DF37B-10DP-0.4V from Hirose. The purpose of the board-to-board connector is to support a future plug-in board featuring an IMU, or an LED board.

The headstage part number, version and revision can be identified from the API. This headstage version has part number NPM_HS_31. Also, the headstage serial number, which is printed on the label and stored on the EEPROM, can be read out.

Table 6 summarizes the key headstage specifications.

Table 6: Key headstage specifications

HEADSTAGE	
SIZE	10 × 14 mm x 3.7 mm
WEIGHT	0.7 g
ZIF CONNECTOR	2 x 17-pin
CABLE CONNECTOR	4-pin (Omnetics)
SOLDER PADS	GND,ELEC_TIP, CAL_SIG (internal imec use)
CONFORMAL COATING	ELPEGUARD / SL 1307 FLZ-T

***NOTE**: Please carefully read and follow the instructions on ESD protection (**Appendix C**) prior to handling any system components.*

The headstage is covered with a layer of conformal coating. Some parts are not covered, to keep electrical contact possible. The area of the headstage which is not covered in conformal coating is indicated in Figure 11 below. ZIF connectors, Omnetics connector, extension board connector and solder pads are not covered.

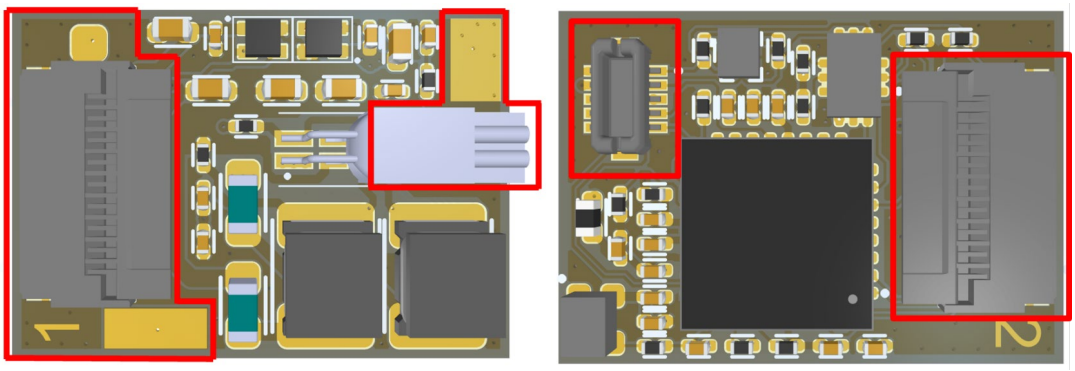


Figure 11: Left: Headstage top side drawing. Right: Headstage bottom side drawing. Areas which are not covered with conformal coating are indicated in red.

3.3 Interface Cable

The Neuropixels single twisted-pair interface cable (Figure 12) provides power from the PXIe acquisition module or OneBox to the HS and transfers control and neural data to/from the HS. The cable assembly weighs 5 g (excl. USB-C connector) and consists of two 5-m long wire strands each having a diameter of 0.41 mm.

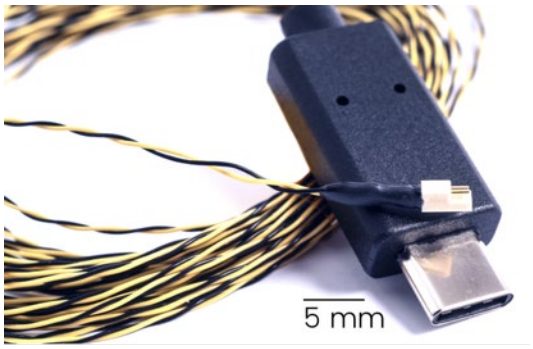


Figure 12: Twisted-pair interface cable with Omnetics-to-USB-C termination.

The HS side of the cable is terminated with a 4-pin Omnetics connector. The PXIe module / OneBox side is terminated with a USB-C connector.

Table 7: Key cable specifications

TWISTED-PAIR DATA/POWER CABLE[7]	
LENGTH	5 m
WEIGHT	5 g (excl. USB-C connector)
DIAMETER	0.41 × 0.82 mm
HEADSTAGE CONNECTOR	4-pin (Omnetics)
PXIE CARD CONNECTOR	USB-C
WIRE STRANDS	1 twisted pair

***NOTE**: Avoid repeated sharp bending of the cable (≤ 2 cm bending radius) as this may degrade cable quality and signal integrity. Use the cable only with the Neuropixels PXIe acquisition module or OneBox; do not plug the cable into any other USB-C port as this may damage the cable.*

3.4 PXIe Acquisition Module

The PXIe acquisition module (Figure 13) is a custom-made board with a deserializer chip and two FPGAs[8] for probe configuration, data acquisition and transmission to PC via a PCIe interface. It is compatible with a standard PXIe chassis, which must be purchased from other well-known third-party vendors such as NI, Keysight or Adlink. Chassis recommendations are provided in Section 2.2 .

[7] Custom cable assembly.

[8] Xilinx ZYNQ and Xilinx Artix-7

The module has 4 USB-C input ports, thus allowing simultaneous connection and operation of up to 4 probes. Various trigger signals[9] can be configured to synchronize and use multiple PXIe modules and thus probes simultaneously.

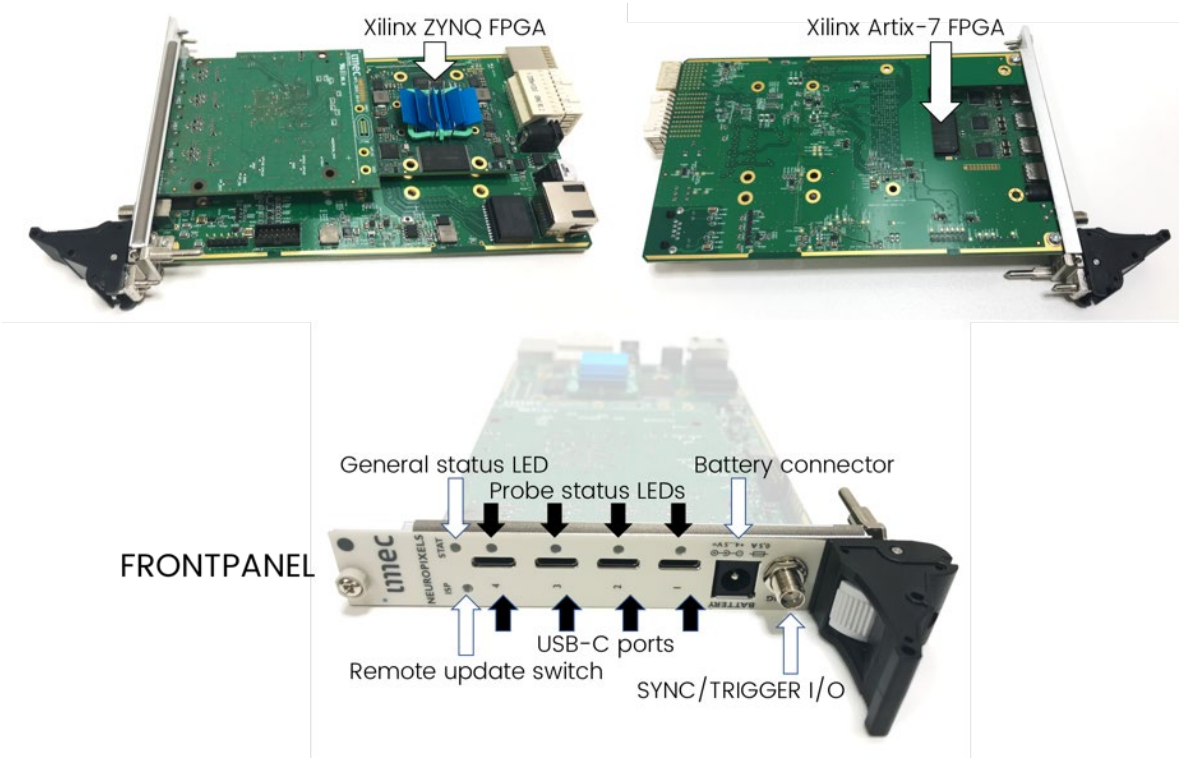


Figure 13: Top: PXIe acquisition module. Bottom: Front panel of the module.

The front panel of the PXIe acquisition module (Figure 13, bottom) contains the following connectors and status LEDs:

- Four numbered USB-C ports allow connection of up to 8 probes. Interface cables can plug into the USB-C port in either orientation.
- An LED next to each USB-C port indicates the status of the respective probe and HS:
  - Off: No clock signal (from a probe) detected. This occurs if the power to the port is not enabled, no probe is plugged into the port, or there is a faulty probe, HS, or cable.
  - Red: The probe is powered on. but errors are observed on the communication channel between probe/headstage and PXIe acquisition module.
  - Green: The probe is powered on and communication between probe and PXIe acquisition module is valid. This is the normal status during operation of the probe.
  - Blue: An internal data emulator on the Artix-7 FPGA is active. The probe data is not used.
- A general status LED indicates the status of the PXIe module:

[9] A trigger line switch matrix and configurable sync clock are implemented. Various trigger signals can be programmed: SMA connector, 7 trigger lines on the PXIe bus, user defined data or software trigger. Common trigger for multiple modules and/or external instruments.

    - Off: The Artix-7 FPGA is not powered, or the boot code is not loaded successfully.
    - Red: Error status related to ZYNQ FPGA or PXIe bus.
    - Green: The Artix-7 FPGA is powered on and the boot code is loaded, waiting for a start trigger to start transmitting neural data.
    - Blue: The Artix-7 FPGA is triggered and is transmitting data to the ZYNQ FPGA.
    - Purple: Combination of red and blue. Data is not read sufficiently fast by the PC. This indicates data loss.
- A switch used for remote updates of the Artix-7 and ZYNQ FPGA boot codes.
- A battery connector to supply power to the probe and HS. The use of this connector is optional. The hardware automatically detects if an external supply is connected and, if so, switches the port supply from internal system supply to external supply. Connect a 4.0-to-5.0 V battery.
- A SYNC/TRIGGER I/O SMA connector:
    - This can serve as an input to connect an external digital trigger signal to start data acquisition, or it can serve as an output to indicate the occurrence of an internal trigger such as a software trigger, a user-defined data trigger, or a trigger from the PXI backplane trigger bus (another PXIe acquisition module or card in the PXIe chassis).
    - It can serve as an input for an external SYNC signal, or it can serve as an output for an internal SYNC signal. This SYNC signal is recorded with neural data across all probes connected to the chassis and can be used to align neural data over different probes in time. When used as an output for the internal trigger signal, a 1 ms pulse is generated on the SMA. When used as an input, a pulse with a minimum width of 16 ns must be connected.
    - The use and polarity of the SYNC/TRIGGER signal is configured using API functions. The SYNC/TRIGGER line is compatible with 5.0 V logic signals. When used as an output (software trigger or SYNC output), a high impedance load must be connected to the SMA connector to observe the SYNC/TRIGGER output.

An EEPROM contains the serial number, part number, version, and revision number of the PXIe acquisition module. While the PXIe module contains hardware provisions for an ethernet connection, neither FPGA code nor API currently support this functionality.

***NOTE**: Please carefully read and follow the instructions on ESD protection (**Appendix C**) prior to handling any system components.*

3.5 OneBox

Coming soon

3.6 Headstage Test Dongle

Coming soon.

4 Installation and Configuration

4.1 PXIe acquisition module control system

This Chapter describes how to install and operate the Neuropixels Control System using a remote controller interface or a Thunderbolt configuration.

4.1.1 Thunderbolt installation

Make sure you have the following hardware components available:

- Third-party PXIe chassis + thunderbolt controller (see Section 2.2 for provider recommendations),
- Desktop or laptop with at least one thunderbolt 3 port.
- Neuropixels PXIe acquisition module (PXIe_1000).

The best installation results were achieved for computers with a preconfigured Thunderbolt port from the factory. Adding a thunderbolt PCIe card to an existing desktop is possible but the card needs to be specifically matched to the motherboard. Matching the manufacturer is not enough to guarantee a successful connection.

The first step is to install the third-party thunderbolt card into your PXIe chassis. Here we will provide you with some basic guidelines but we do emphasize the need to follow the instructions and safety information described in the user manuals of the chosen PXIe chassis and remote controller provider.

Follow the steps below to install the PXIe-8301 thunderbolt card into the NI PXIe-1071 chassis and connect the thunderbolt cable to the PC:

1. Power-off the PXIe chassis but leave the power cable plugged in to ground the chassis.
2. Identify a valid PXIe slot and remove the filler panel. The slot type on the chassis can be identified by symbols next to the slot number, as shown in Figure 17. The PXIe-8301 thunderbolt module must be plugged into the 'PXIe Controller Slot'.

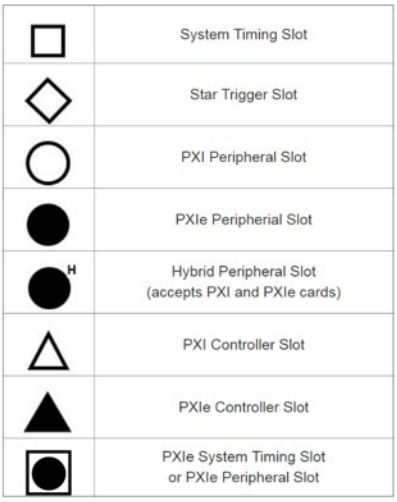


Figure 14: PXIe chassis slot symbols (source: ni.com).

3. Push the ejector handle down (Figure 18) by pressing the grey button (step 1) on the handle and subsequently pushing the black handle (step 2) down.

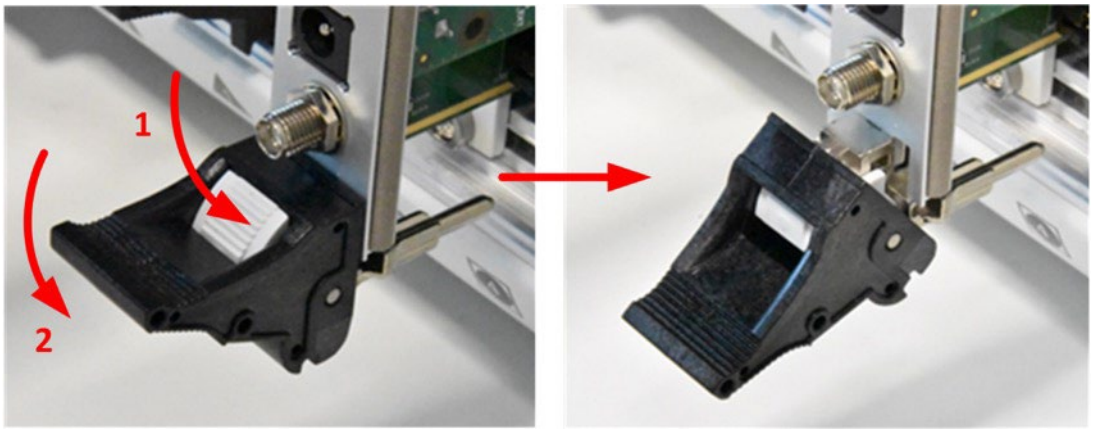


Figure 15: Push the ejector latch down prior to inserting the module.

4. Slide the module into the PXIe slot. Observe the correct orientation of the module. When the ejector handle touches the metal rail of the chassis, lift the ejector handle to push the module into the slot for the last few millimeters.

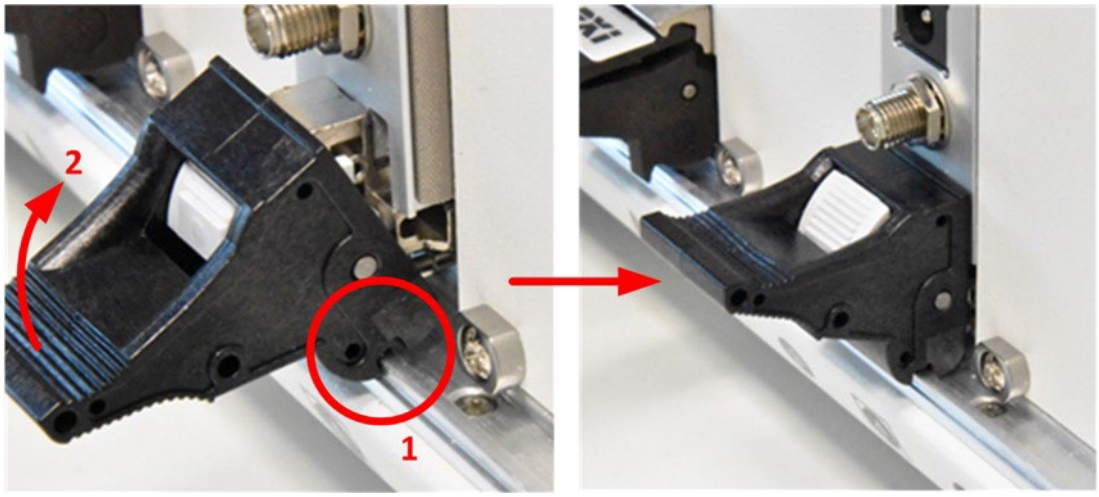


Figure 16: Push the ejector latch up to plug the BS module into the backplane connectors.

5. Secure the PXIe module with the mounting screws on the front panel.
6. Plug one side of the thunderbolt cable in the thunderbolt port of the PXIe 8301 module and connect the other side to a thunderbolt port on the PC. (Warning: make sure the thunderbolt cable is connected to a thunderbolt port and not a standard USB-C port.)
7. Update the BIOS firmware of the PC in case this is not the latest version.
8. Install the latest Thunderbolt drivers in case the standard thunderbolt driver is missing.
9. Power off the PC.
10. Continue with step 14 in section 4.1.3 on page 28.

4.1.2 PXIe Chassis and Remote Controller

This section describes how to install and operate the Neuropixels Control System using a PXIe chassis and Remote Controller. Make sure you have the following hardware components available:

- Third-party PXIe chassis + remote controller (see **Section 2.2** for provider recommendations),
- PC with at least one PCIe slot (Gen 2 x8 or wider) (see Section 2.2 for additional hardware and system requirements; also consult the requirements for the application software you intend to use)
- Neuropixels PXIe acquisition module (PXIe_1000).

The first step is to install the third-party remote controller into your PXIe chassis. Here we will provide you with some basic guidelines but do emphasize the need to follow the instructions and safety information described in the user manuals of the chosen PXIe chassis and remote controller provider.

Follow the steps below to install the PXIe-8398 remote controller into the NI PXIe-1071 chassis and the NI PCIe-8398 board into the PC:

1. Power-off the PXIe chassis but leave the power cable plugged in to ground the chassis.

2. Identify a valid PXIe slot and remove the filler panel. The slot type on the chassis can be identified by symbols next to the slot number, as shown in Figure 17. The PXIe-8398 remote control module must be plugged into the 'PXIe Controller Slot'.

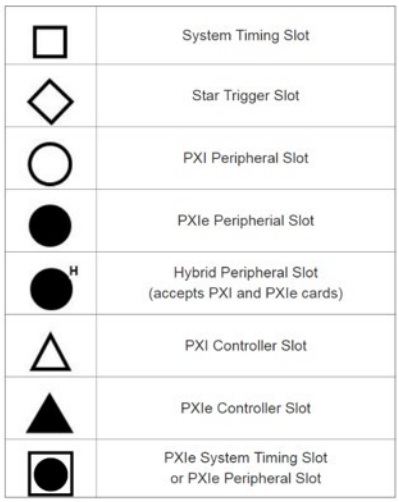


Figure 17: PXIe chassis slot symbols (source: ni.com).

3. Push the ejector handle down (Figure 18) by pressing the grey button (step 1) on the handle and subsequently pushing the black handle (step 2) down.

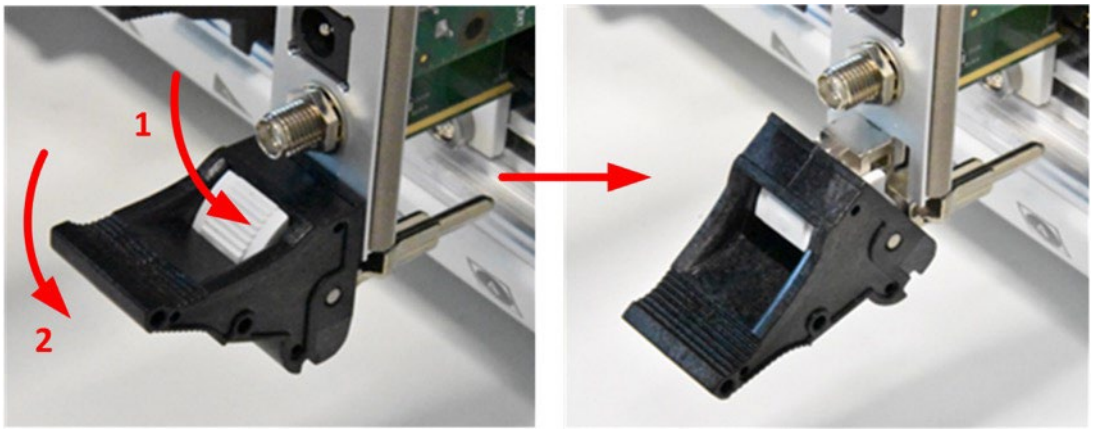


Figure 18: Push the ejector latch down prior to inserting the module

4. Slide the module into the PXIe slot. Observe the correct orientation of the module. When the ejector handle touches the metal rail of the chassis, lift the ejector handle to push the module into the slot for the last few millimeters.

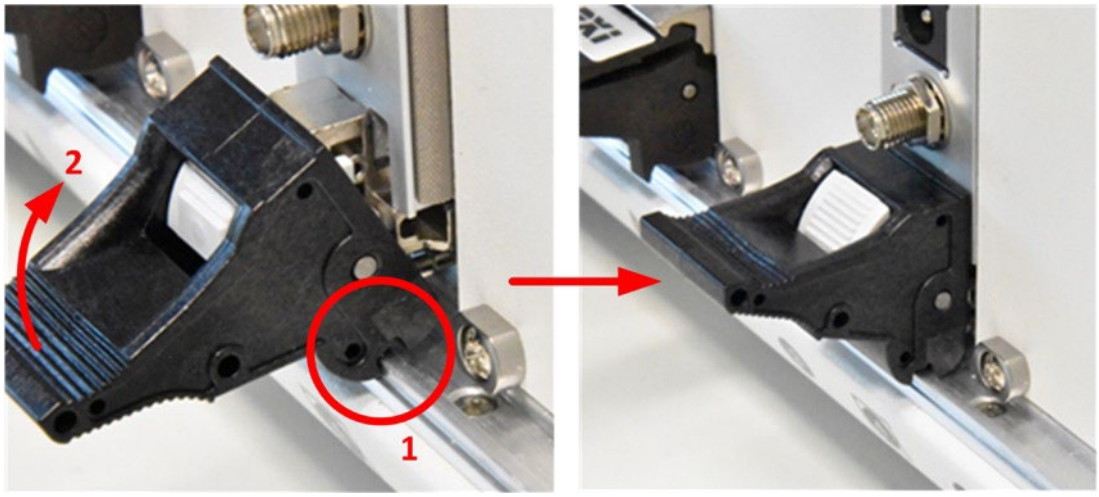


Figure 19: Push the ejector latch up to plug the BS module into the backplane connectors

5. Secure the PXIe module with the mounting screws on the front panel.
6. Power off and unplug your host computer.
7. Remove the top cover or access port to the PCIe expansion slots.
8. Select any available PCIe x16 expansion slot (Figure 20).
9. Locate and dislodge the metal bracket that covers the cut-out in the back panel of the computer for the slot you have selected.
10. Insert the PCIe-8398 board into the expansion slot (Figure 21).
11. Secure the metal bracket back in place.
12. Replace the computer cover.
13. Connect the MXI-Express x16 cable to both MXI-Express x16 cards. The cables have no polarity, so you can connect either end to either card.

Continue with step 14 in section 4.1.3.1 further below.

Figure 20: PCIe x16 slot on the PC motherboard.

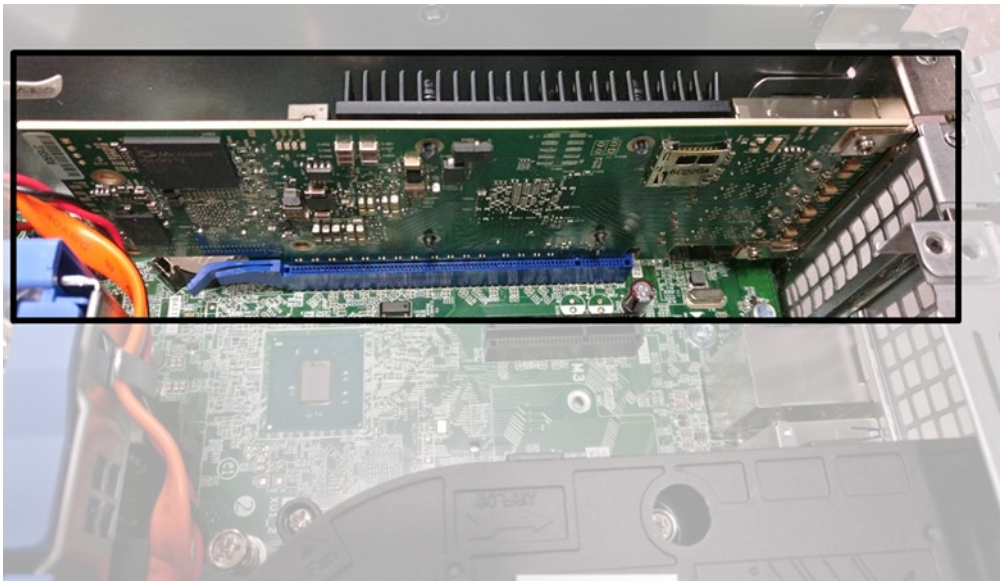


Figure 21: NI PCIe-8398 board plugged into the PC.

4.1.3 Neuropixels Hardware

All Neuropixels system hardware is delivered preconfigured by imec. No further configuration is required. An update procedure is available for the PXIe acquisition module in case an update of the FPGA firmware code is required. The full procedure to update the FPGA firmware is described on the website of SpikeGLX.

4.1.3.1 PXIe Acquisition Module

Continue with the steps below to install the PXIe acquisition module into the chassis:

14. Ensure the PXIe chassis and host PC are still powered off.
15. Identify a valid PXIe slot in the chassis and remove the filler panel. The slot type on the chassis can be identified by symbols next to the slot number, as shown in Figure 17. The PXIe acquisition module must be inserted into a 'PXIe Peripheral Slot', 'Hybrid Peripheral Slot' or 'PXIe System Timing Slot'.
16. Follow the same steps 3-5 as above.
17. Power on **first** the PXIe chassis and **then** the host computer (in this sequence). The global status LED on your PXIe acquisition module should switch from red to green as shown in Figure 22. The 'LINK' status LED of the remote controller will also turn green.

Figure 22: Global status LED of the PXIe acquisition module switching from red to green after correct installation.

4.1.3.2 Drivers

After mounting the PXIe acquisition module into the chassis, install the Enclustra FPGA driver files that you have downloaded as described in **Section 2.3**.

A detailed procedure with screenshots on how to install the driver on a Windows 10 machine is given below.

1. Start the Windows Device Manager with an administrator account. The example in the screenshot below shows the device manager for a chassis with one base station plugged in, prior to installation. The PXIe acquisition modules show up as **PCI Memory Controller** under **Other devices**.

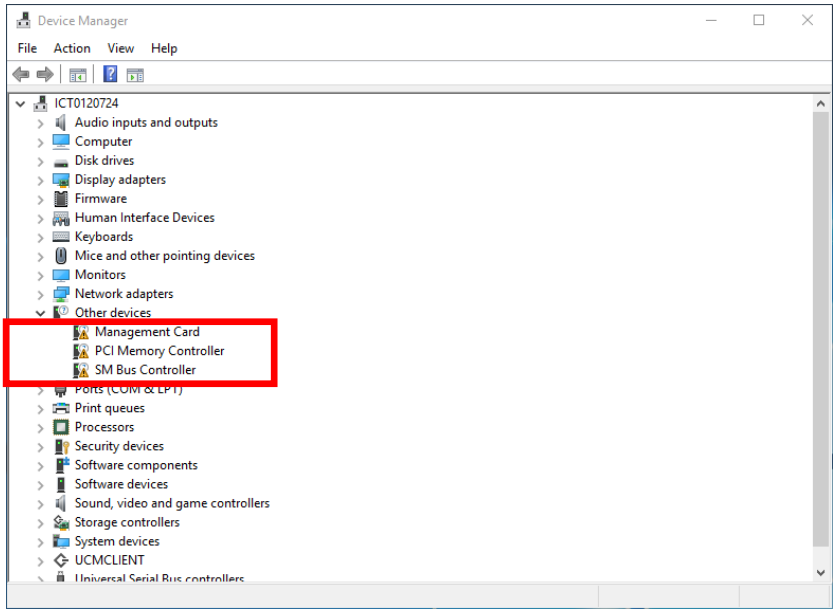


Figure 23: Windows 10: Device Manager before driver installation.

2. Right click 'PCI Memory Controller'. Click 'Properties'.
3. Click 'Change settings'

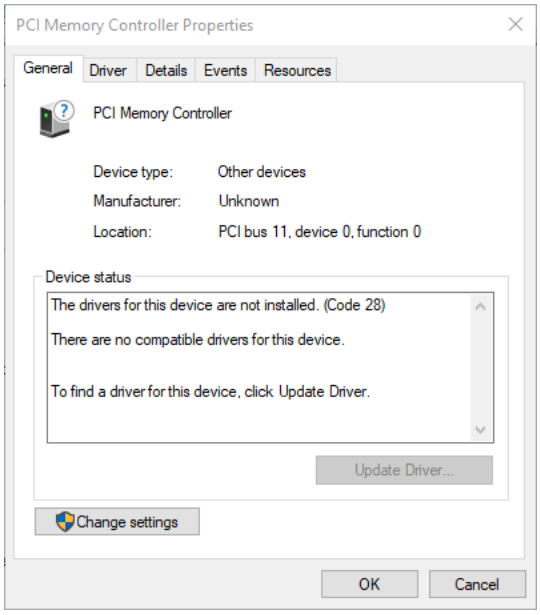


Figure 24: Windows 10: Uninstalled device properties.

4. Click 'Update Driver...'

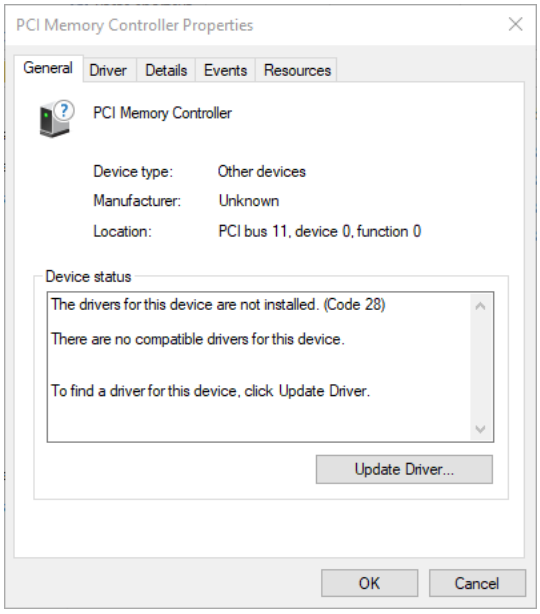


Figure 25: Windows 10: Editable device properties.

5. Click 'browse My computer for driver software'

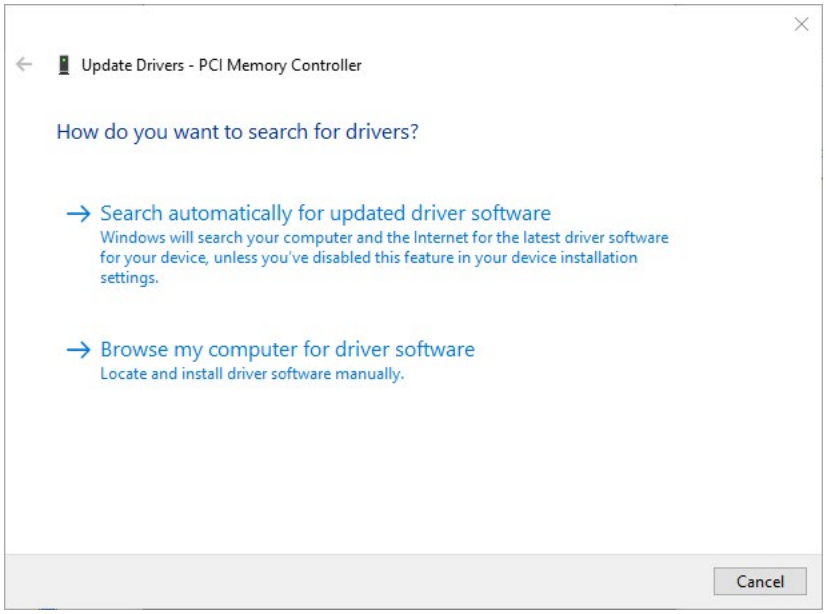


Figure 26: Windows 10: Install driver.

6. Browse to the location with the driver files. Click 'Next'.

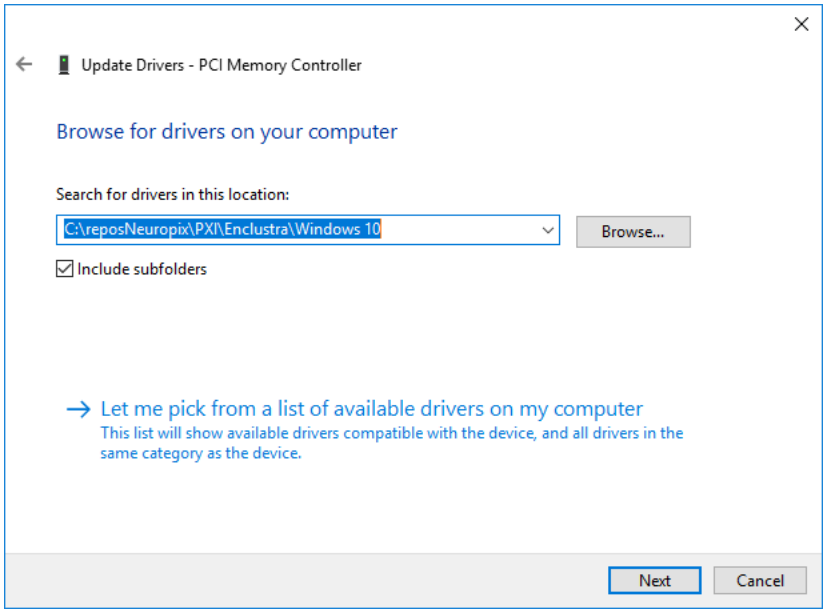


Figure 27: Windows 10: Select driver file.

7. If all goes well, you get a screen saying that Windows has successfully updated your driver. Click 'Close'.

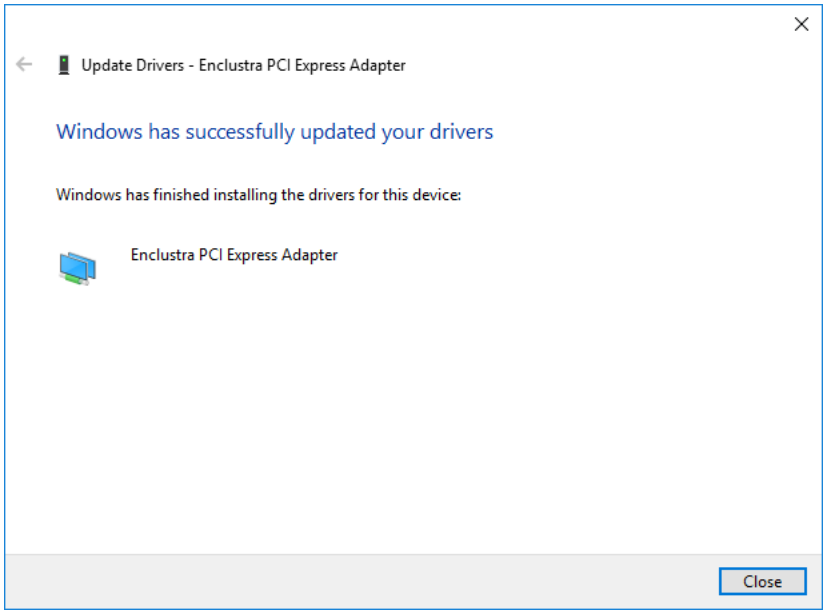


Figure 28: Windows 10: Successful driver update confirmation.

8. Click 'Close'.

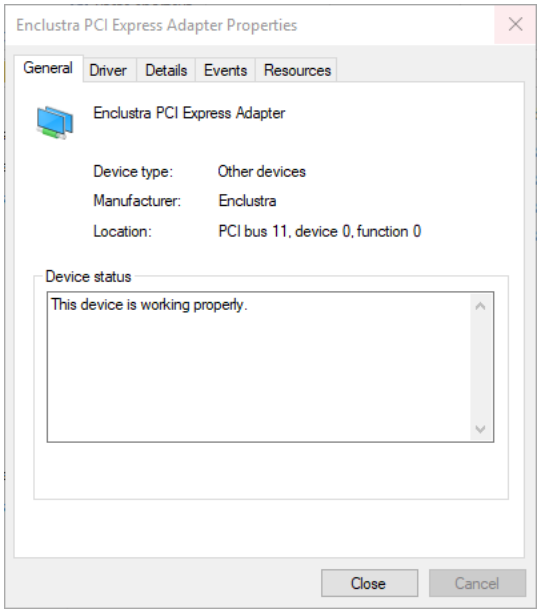


Figure 29: Windows 10: Device properties after installation.

9. Reboot the PC and log in with a normal user account. Check the installation of the driver in the Device Manager. After successful installation, an **Enclustra PCI Express Adapter** shows up in the **Device Manager** under **Enclustra Devices**.

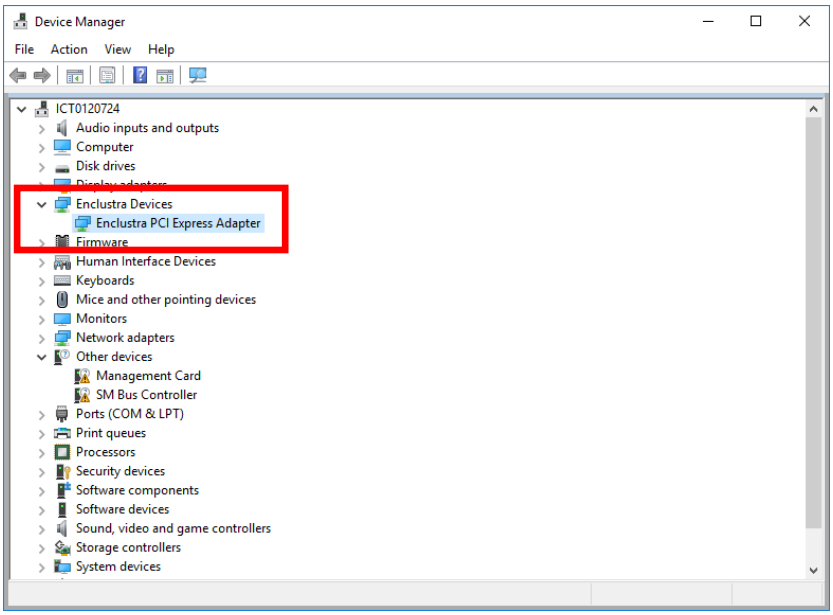


Figure 30: Windows 10: Device manager after installation.

To start Windows 10 in safe mode or get to other startup settings:

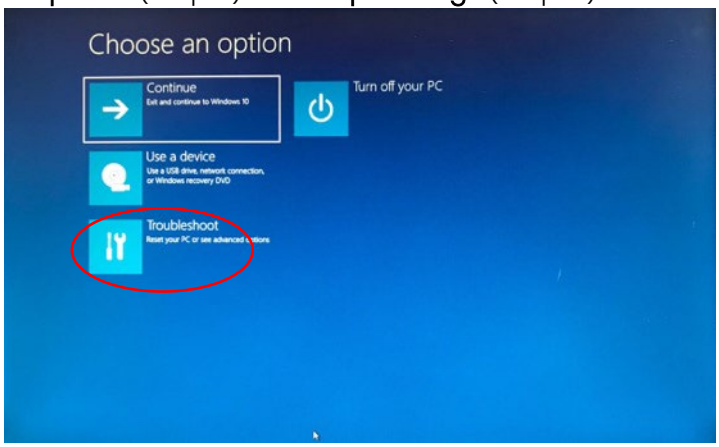
1. Select the **Start** button, then choose **Settings**
2. Select **Update & security** > **Recovery**.
3. Under **Advanced startup** select **Restart now**.

4. After your PC restarts to the **Choose an option screen** (step 1 below), select **Troubleshoot** (step 2) > **Advanced options** (step 3) > **Startup Settings** (step 4) > **Restart**.
5. After your PC restarts, select '**7**' or '**F7**', your PC will automatically reboot with the new startup setting.

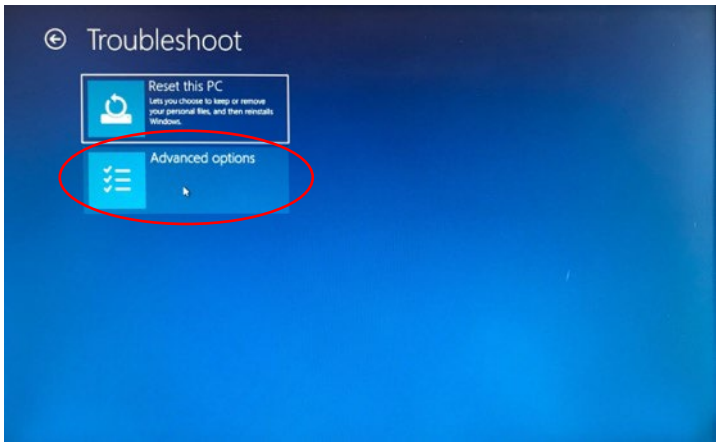
Alternatively, you can get to the startup options form the sign-in screen:

1. On the sign-in screen, hold the **Shift** key down while you select **Power** > **Restart** (in the lower-right corner of the screen).
2. After your PC restarts to the **Choose an option** screen, select **Troubleshoot** (step A) > **Advanced options** (Step B) > **Startup Settings** (Step C) > **Restart** (Step D).

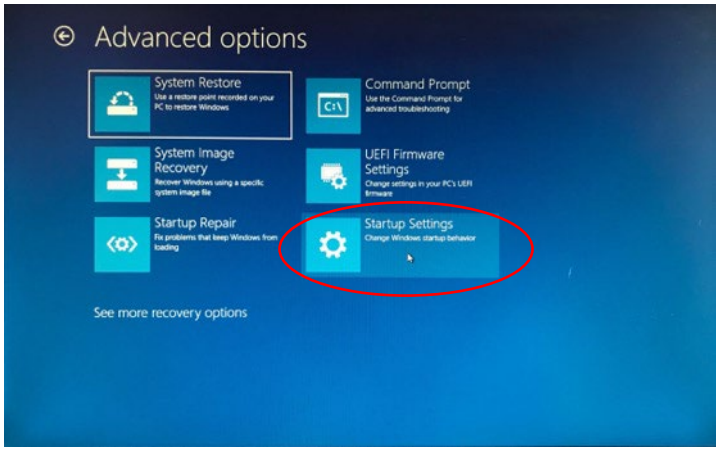
STEP A



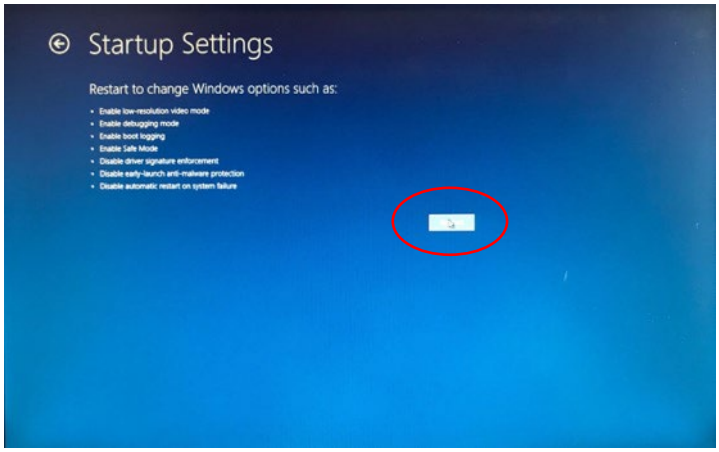
STEP B



STEP C

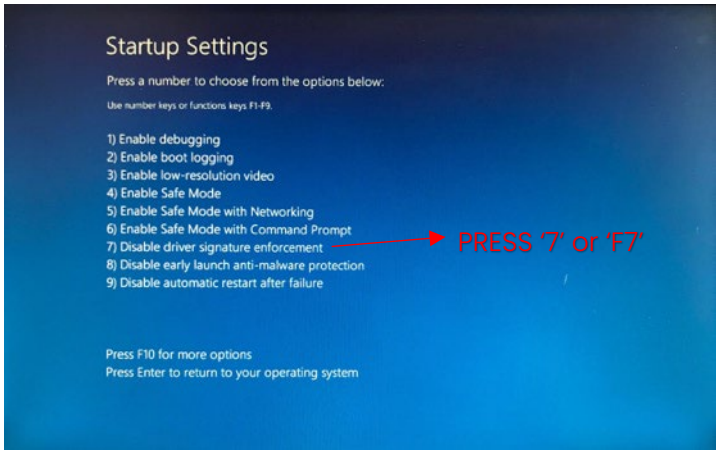


Step D



3. After your PC restarts, press '**7**' or '**F7**' (Step E), your PC will automatically reboot with the new startup setting.

Step E



An unsuccessful installation of the driver can also be fixed by uninstalling and reinstalling the driver.

4.1.3.3 Remote FPGA update

The PXIe acquisition module is shipped with firmware programmed on the board. However, firmware updates which extend the functionality of the PXIe acquisition module will be released. Updating the firmware on the board can be done with the application software packages SpikeGLX or Open Ephys. However, in case this update procedure would fail, for example due to a power failure of the system during the update process, a recovery procedure needs to be followed:

- If the PXIe chassis has not been switched off after the firmware update procedure has failed, you can simply repeat the update procedure from the application software.
- If the PXIe chassis has been switched off after an unsuccessful firmware update, you need to press and hold the ISP switch on the front panel of the PXIe acquisition module during powering on of the PXIe chassis. You can use a pen to press the switch. Keep the switch pressed for a few seconds, until the STATUS led lights up as green. The update procedure can now be repeated from the application software.

4.2 OneBox

Coming soon

5 Using the System

5.1 Connecting the System Components

5.1.1 Probe to HS

The probe flex connects to the HS via the ZIF connector (Figure 31, right). To plug the flex into the HS, gently lift the black latch of the HS ZIF connector. The flex needs to be plugged in the headstage ZIF connector with the golden contacts at the flex ZIF side facing down and the ZIF connector on the headstage facing up (Figure 32 and Figure 33). Ensure that the flex cable is fully inserted into the HS ZIF connector before closing the connector latch. It is best to close the latch while maintaining slight pressure to keep the flex seated; a good connection is crucial for the recording. In case you are not able to record from a probe please try to reseat the probe flex into the headstage. Insert the flex as deep as possible in the zif connector and maintain force on the flex while closing the black lid.

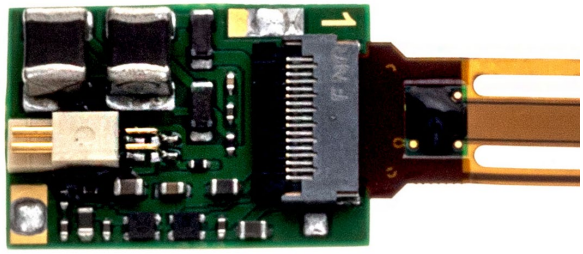


Figure 31: Headstage with probe inserted in front side ZIF connector

Figure 32: Correct way to plug the flex in the ZIF connector. Top: front side dock, Bottom: back side dock

Figure 33: Wrong way to plug the flex in the ZIF connector. Top: front side dock, Bottom: back side dock.

5.1.2 HS to PXIe Acquisition Module or Onebox

The PXIe side of the interface cable is terminated with a USB-C connector, which is symmetric and can thus be plugged into the PXIe acquisition module or OneBox in either orientation. The HS side of the cable is terminated with a 4-pin Omnetics connector. This connector is not symmetric and must be plugged into the HS so that the two exposed metal pins mate easily with the two receiving holes (Figure 10 on page 18, left).

***NOTE**: Please carefully read and follow the instructions on probe handling (**Appendix A**) and ESD protection (**Appendix C**) prior to handling any system components.*

5.2 Probe and System Configuration

The Neuropixels API provides various functionalities to control, configure and test the probe and control system, including (but not limited to):

- Selection of recording electrodes, reference inputs, channel gains, and bandwidth.
- Selection of trigger mode.
- Loading of probe-specific configuration files (these files are provided by imec with every probe shipment through a file transfer service. In case you lost the calibration files please contact neuropixels.sales@imec.be.)
- Reading of serial numbers, part numbers, hardware versions, and software versions.
- Enabling of BISTs.
- and others.

Most of these functions are already implemented in the application software packages mentioned in **Section 2.4.1** and are described in the respective online *User Manual* and *Documentation*.

Below, we will briefly describe the electrode selectivity and reference selection.

5.2.1 Electrode Selectivity

Each of the 4 shanks has 1280 electrodes. The base has 384 channels. Since the shank has 1280 electrodes and the base 384 channels, there are 3 1/3 virtual banks of 384 electrodes in the shank (Figure 34). Therefore, each channel can connect to 3 or 4 electrodes.

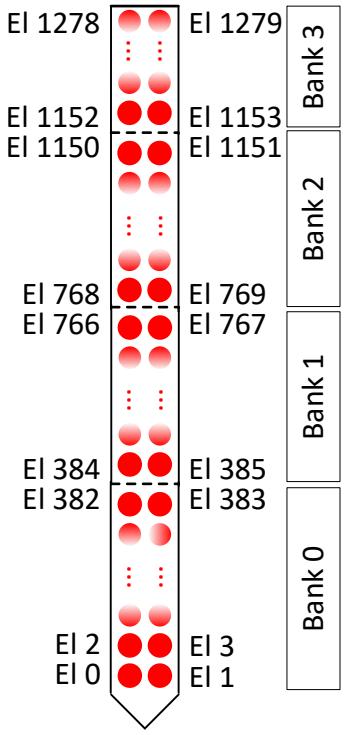


Figure 34: Electrode bank distribution along the shank.

No channel scrambling is implemented on the multi-shank probe. Each of the 4 shanks has a different electrode-channel mapping. Each channel can connect to only one electrode: connecting a channel to more than one electrode on the same shank or over different shanks is not enabled. Examples are given in Figure 35. The electrode-channel mapping for the multi-shank version is described in Neuropix_2_0_Multi-Shank_Electrode-Channel-mapping.xlsx.

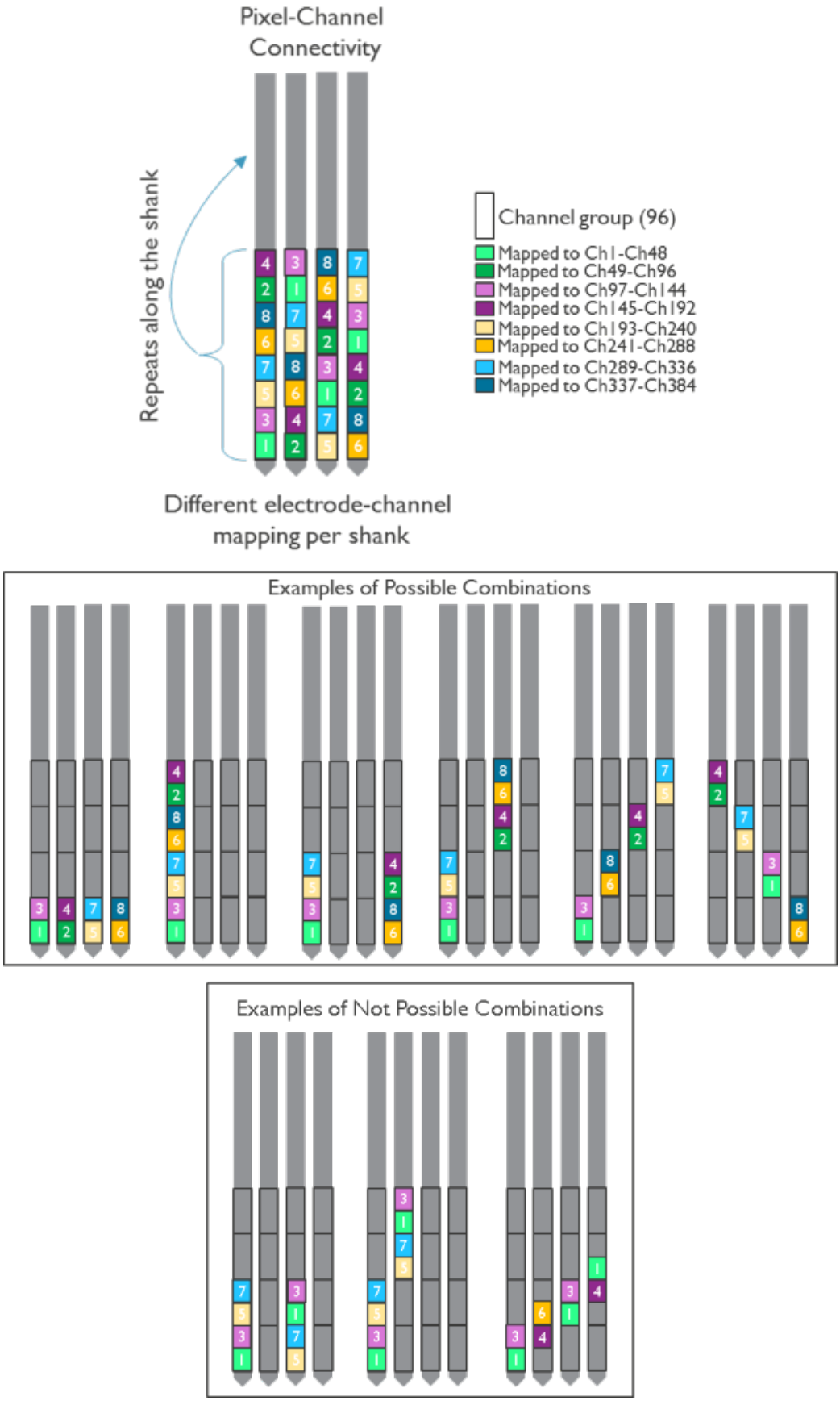


Figure 35: Electrode-channel connectivity in the multi-shank probe.

5.2.2 Reference Selection

Three reference inputs are available for each channel:

- External reference: multiple input pads are located on the probe flex. Separate wires can be soldered to these pads.
- Tip electrode: a large TiN electrode located at the tip of each shank.
- Ground reference: the reference input is connected to the ground of the ASIC. This selection is an alternative for shorting the reference and ground pads on the flex arms. This configuration is intended to replace the use case where the user is shorting reference and ground on the flex arms by soldering. The reference selection is channel-independent, and each channel can only connect to one of the three reference inputs simultaneously.

5.3 Support and Troubleshooting

Neuropixels probes are provided to the neuroscience research community at low cost on a non-for-profit basis. All technical and user support is based on a community support model.

To learn how to use the Neuropixels probe and control system, new users are encouraged to attend one of the regularly organized user workshops or training courses prior to using the probes. Courses are currently offered by University College London through a grant by the Wellcome Trust and generously supported by the Sainsbury-Wellcome Centre.

If your Neuropixels probes appear to malfunction and not perform to specifications, we encourage you to:

- Carefully read this *User Manual*.
- Take advantage of the growing knowledge base shared on various online collaboration platforms: The Neuropixels Slack channel and a GitHub Wiki. In addition, both SpikeGLX and Open Ephys are helpful information sources. A list of available web-based resources is available at www.neuropixels.org.

In the unfortunate event that your probe is defective and/or non-functional, you may contact neuropixels.info@imec.be or neuropixels.sales@imec.be to discuss a suitable remedy and process to make sure that you have functional Neuropixels probes. This will be the fastest and most efficient mechanism for you to resolve issues with your Neuropixels probes. Please do not contact imec directly at any of the generic imec email contact information addresses.

In the following we describe various tests that you can perform to identify the root cause of observed failures.

5.3.1 Visual Inspection

Inspect your probe and system components for visible defects. The probe shank should also be inspected under a microscope to determine possible debris contamination or physical damage such as scratches.

5.3.2 Built-In Self-Tests

As good practice you should start debugging your probe and/or control system by first running the BISTs which must be enabled in the application software. The results will indicate the type and location of possible failures modes. On system level, these tests verify whether all power and data links are functional and whether data integrity criteria are met. On probe level, these tests verify the correct programming of and data streaming from the probe ASIC, thus assessing functionality and performance of the electrodes and integrated electronics.

To run a BIST test in SpikeGLX follow the instructions below:

- Connect a probe with a headstage and cable to the PXIe data acquisitioning module or OneBox.
- Open SpikeGLX
- Go to the menu "TOOLS" => "BIST (Imec probe diagnostics)…"
- Select the correct Slot, Port and Dock and press "Go". This will run all defined tests by default.

Be aware the noise test may fail since you are testing the probe in suboptimal conditions.

5.3.3 Headstage Test Dongle

Coming soon

5.3.4 Gain and Noise Measurements

The functionality and performance of a probe can also be verified with a simple gain and/or noise measurement in PBS solution. These measurements should be performed after loading the probe configuration files into the software.

Gain measurements must be performed using the external REF shorted to GND. This can be achieved by soldering two wires to the respective pads on the probe flex and shorting them to a signal generator's ground (Figure 36). A sinusoidal test signal of e.g. 5 mV_{pp} and 1.0 kHz or 100 Hz, for AP or LFP band, respectively, can be applied to the PBS using a Pt, stainless steel or Ag|AgCl counter electrode. The resulting mean gain should not deviate >10% from the nominal value (x100) and at least 90% of the electrodes should have a gain within 5% of the mean gain. The results can provide qualitative and quantitative information about electrodes and/or channel performance.

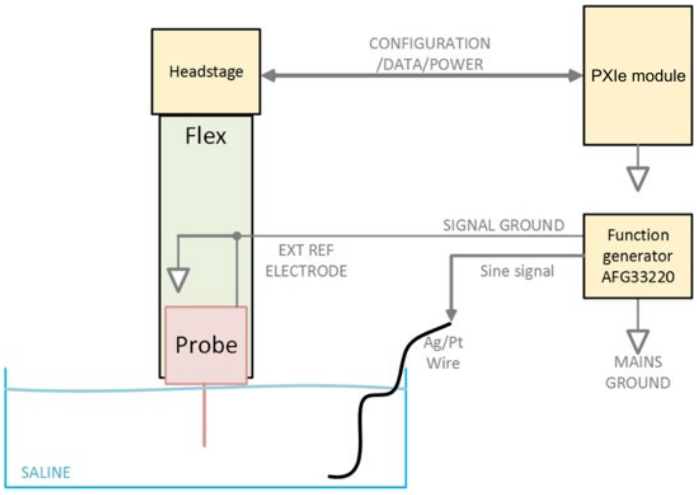


Figure 36: Setup for gain measurements in PBS.

Noise measurements should always be performed in a grounded Faraday cage. Like for gain measurements, noise measurements must be performed using the external REF shorted to GND. The reference selection is done via the GUI. The PBS solution must be grounded (Figure 36). During noise measurements, all electrodes must be immersed in PBS to avoid unwanted noise pick-up and cross-coupling.

To obtain the actual input-referred noise, one must divide the measured noise by the actual gain measured with the gain measurement procedure.

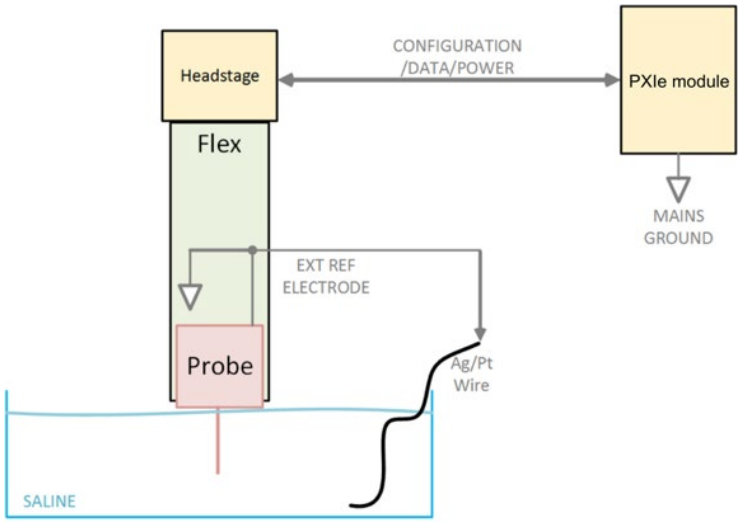


Figure 37: Setup for noise measurements in PBS.

5.3.5 Frequently asked questions

Q1: What is the purpose of the dummy probes? Are they electrically functional?

A1: Dummy probes are physically the same as functional probes but are not able to be recorded from; they are not electrically functional. We provide users with dummy probes for mechanical tests and practice purposes. Dummy probes come in sets of 6pc/ box and can be ordered from the Order page on the Neuropixels website.

Q2: What is the difference between a probe with a cap and a probe without a cap?

A2: Every type of probe created by Neuropixels comes in silicon- and metal-capped versions. A probe without a cap refers to the silicon version; a probe with a cap refers to a probe with an aluminum metal cap and dovetail-shaped attachments. This type of probe connects to a dedicated probe holder designed by HHMI. The purpose of the HHMI holder is to ease probe insertion or to facilitate acute recordings. You can consult the design via this link.

If you would like to use the HHMI holder, you must order the metal-capped probe and the probe holder separately (the metal caps themselves are not available for individual sale).

On the RFQ form, the HHMI holder is titled "HOLDER_2000_C".

A probe without a cap refers to those with silicon spacers on top of the ASIC. These probes are not usable with the HHMI holder. Some labs prefer this type because they prefer a custom attachment, or they would like to insert the probes closer together.

Please have a look at the website for more information.

Q3: What is the cost of the recording software and where can I get it?

A3: The Neuropixels software to record is open source and provided free of cost by SpikeGLX and/or OpenEphys. This software can be downloaded free of cost. Please visit following website for more information:

- https://billkarsh.github.io/SpikeGLX/
- https://open-ephys.github.io/gui-docs/User-Manual/Plugins/Neuropixels-PXI.html#neuropixelspxi

Q4: How can I become a member of the dedicated Neuropixels Slack channel?

A4: Please subscribe using following link:

- https://join.slack.com/t/neuropixelsgroup/shared_invite/zt-2c8u0k21u-CC4wSkb8~U_Fkrf3HHf_kw

Q5: I want to place an order for probes and system parts. How do I proceed?

A5: Please download the RFQ form on the website . Fill in all the details and quantities and send the document to neuropixels.sales@imec.be . They will provide an official quotation which needs to be signed.

Q6: What's the standard lead time for products?

A6: The standard lead time is 120 days. The orders will be shipped sooner if possible.

Q7: I lost my calibration files. How can I retrieve them?

A7: Please send an email to neuropixels.info@imec.be or neuropixels.sales@imec.be. The calibration files will be sent to your email address.

Q8: The imec data acquisition card PXIe_1000 does not show up in the NI MAX tool?

A8: It's correct that the imec data acquisition card does not show up in the NI MAX tool. This does not mean that the card is dysfunctional.

Appendix A Probe Handling, Cleaning, Storage

Please follow these guidelines to remove the probes from the shipping box:

- Wear gloves to minimize dust and dirt contamination. Work in a clean environment.
- Carefully open the box with the lid pointing away from you. Make sure the lid stays upright.
- Remove the complete foam from the carton box (Figure 38 and Figure 39).
- Carefully lift the top foam from the bottom foam, which contains the probes (Figure 39).
- Up to six probes are shipped in each box.
- We advise removing probes only from the leftmost non-empty slot not to accidentally touch the other probes.

Figure 38: Removing the probes in the foam from the carton shipping box.

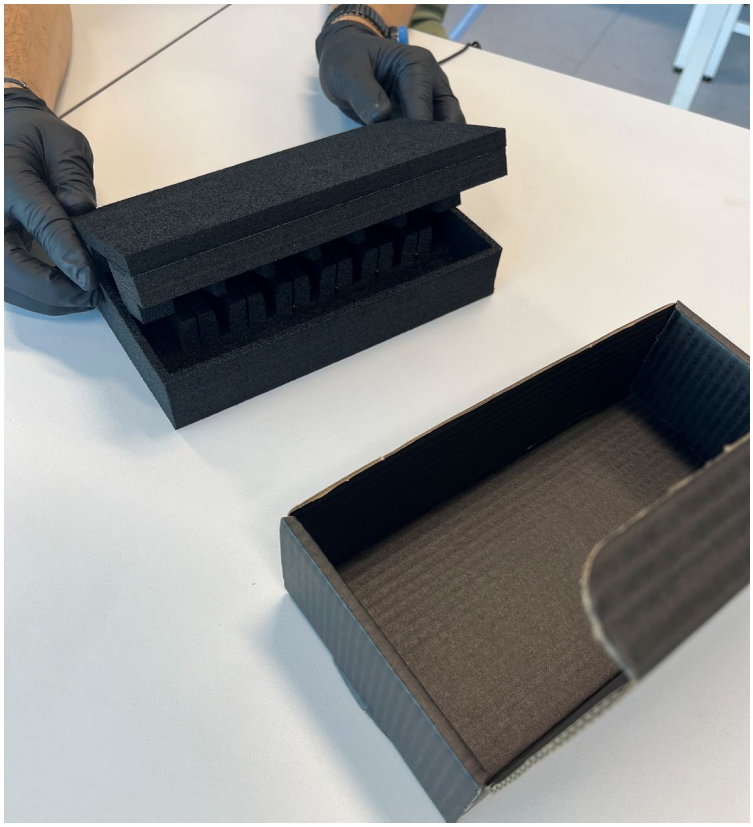


Figure 39: Removing the foam from the carton box and lifting the top foam.

With one hand, push the foam holding a probe open to make space for the probe to be taken out (Figure 40).

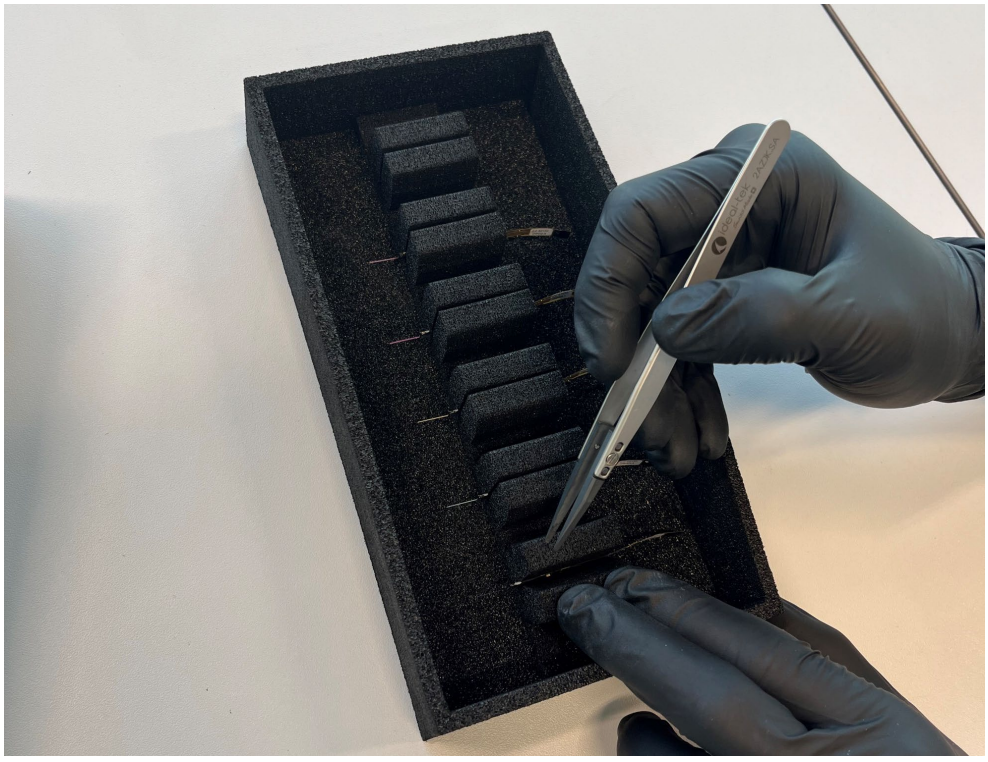


Figure 40: Removing the probe from the foam.

- Take a pair of ESD-safe tweezers and carefully clamp the base of the probe as shown in Figure 41.
- Carefully pick up the probe while keeping the foam pushed open.
- At all times, keep your eyes on the shank and make sure that it does not touch the foam.

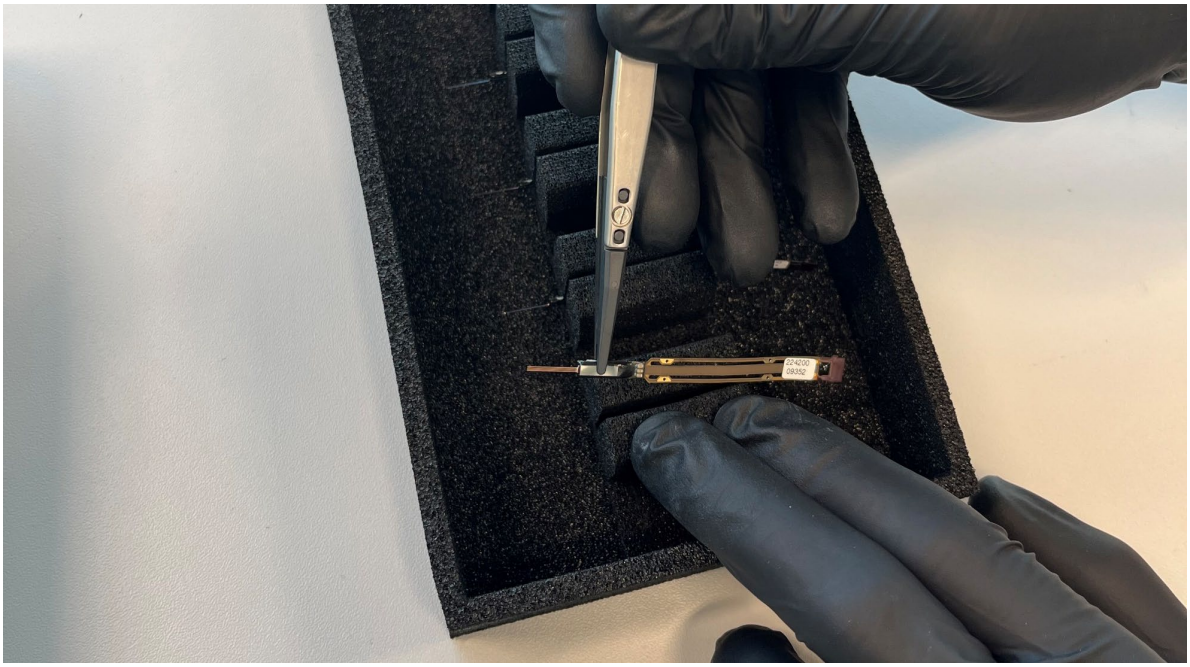


Figure 41: Removing the probe from the foam by clamping the base with tweezers.

Please follow these guidelines to ensure mechanical integrity of the fragile shank, electrodes and flex:

- Do not touch the shank with your fingers or other objects.
- Do not subject the probe to vibrations (potential damage of TiN electrodes and shank). Such vibrations could arise e.g. when blow-drying the probe with compressed air or N_2 or when subjecting the probe to ultrasound.
- Always work in a clean environment and wear gloves.
- Regularly inspect the probes with an optical microscope to verify that shank and electrodes are undamaged and clean. Color changes/darkening of the TiN can indicate corrosion or other damage. Please report such observations.
- Do not pinch the flex of the probe and maintain a minimum bending radius of 3 mm.
- Store the probes in the black ESD safe shipping boxes at room temperature.

Follow these cleaning guidelines:

- Strong oxidizing agents (acids, bases, H_2O_2, etc) and/or elevated temperatures (>100 °C) should be avoided as these may irreversibly deteriorate the TiN electrode impedance and thus noise. The following treatments and solutions have been tested and are safe to use with Neuropixels probes (no other organic solvents should be used):

    - Deionized water (DIW)[10] at room temperature
    - Iso-propyl alcohol (IPA)
    - Phosphate buffered saline (PBS) @ pH 7.4 (https://www.sigmaaldrich.com/content/dam/sigma-aldrich/docs/Sigma/Datasheet/pbs1dat.pdf)
    - 25 mM MOPS (3-(N-morpholino)propanesulfonic acid) (http://www.sigmaaldrich.com/catalog/product/sigma/m1254?lang=en&region=BE), 150 mM NaCl, DI water, pH adjusted w/ NaOH and HCl
    - 100 mM MES (2-ethanesulfonic acid) (https://www.sigmaaldrich.com/BE/en/product/fluka/69889), 150 mM NaCl, DI water, pH adjusted w/ NaOH and HCl
    - Tergazyme (http://www.sigmaaldrich.com/catalog/product/aldrich/z273287?lang=en&region=BE)
    - Ethylene oxide gas sterilization

- When performing experiments in PBS, avoid submersing the electric components into the PBS. While coated with a conformal coating, full hermeticity cannot be guaranteed. Immediately rinse with DIW and IPA and re-test the probe.
- After use in PBS, always rinse the probes (including the electrical components) under a gentle DIW stream or in a beaker for 1-2 minutes followed by IPA rinsing for 1-2 minutes. Do not use a high-pressure water or IPA stream. After IPA rinsing, you can let the probes dry in air. The use of IPA is not mandatory but advised.
- Avoid leaving the probes dry out after removal from PBS. Salt crystals may form on the shank and TiN electrodes that are difficult to remove.
- Always use fresh solutions, i.e. don't use beakers with DIW, IPA, or PBS after prolonged exposure to air (~1/2 day) since dust particles on the liquid surface may irreversible attach to the shank surface when immersed or rinsed with these solutions.
- After *in-vivo* use, soak the dirty probes in PBS until ready to clean them. Letting the shank dry out makes the cleaning less effective. Follow these cleaning steps:
    - Prepare 1% Tergazyme solution.
    - Soak the explanted probes in standard PBS (pH 7.4) until cleaning with Tergazyme (to prevent drying out).
    - Immerse probes in Tergazyme solution @ RT (12h soaking on shelf).
    - Thoroughly rinse with DIW (~5 min under gentle DIW stream); if soaking in DIW is used, a brief rinse with DIW should be applied at the end.
    - Rinse the probes with IPA and let it dry in air.

Store the probes in the black ESD safe shipping boxes at room temperature.

[10] Rinsing or prolonged soaking of Neuropixels probes in DIW (pH ≈ 5.7) does not deteriorate the TiN impedance; if anything, the impedance slightly decreases after prolonged soaking (likely due to improved wetting). DIW degassing is not needed.

Appendix B Soldering

If the experiment requires a connection to the ground and/or external reference signal, the user can make use of the two GND and REF arms which are part of the probe flex. In case these arms are not usable as such, the user can extend or replace these by soldering wires to the provided solder pads on the flex. Two solder pads are available for both GND and REF connection. These solder pads are reinforced with blind vias to prevent peel-off of the solder pads from the flex.

A well-maintained solder iron makes soldering to the probe much easier. Below are some general guidelines to keep your solder tips in good condition:

- Set the temperature of the solder iron to the minimum required for the application.
- Apply some solder to the solder tip before switching off. This prevents corrosion to the tip.
- Switch off the solder station or unplug the solder iron from the station when not in use.
- Replace the tip when the solder wire does no longer melt on the very tip of the solder tip.
- Always choose a solder tip which matches the size of the solder pad as good as possible.

Solder procedure:

- Make sure to use a solder iron which is grounded via the mains supply of the soldering station for ESD protection.
- Fix the probe to a clean surface. A good method is to use ESD tape. (Figure 42)

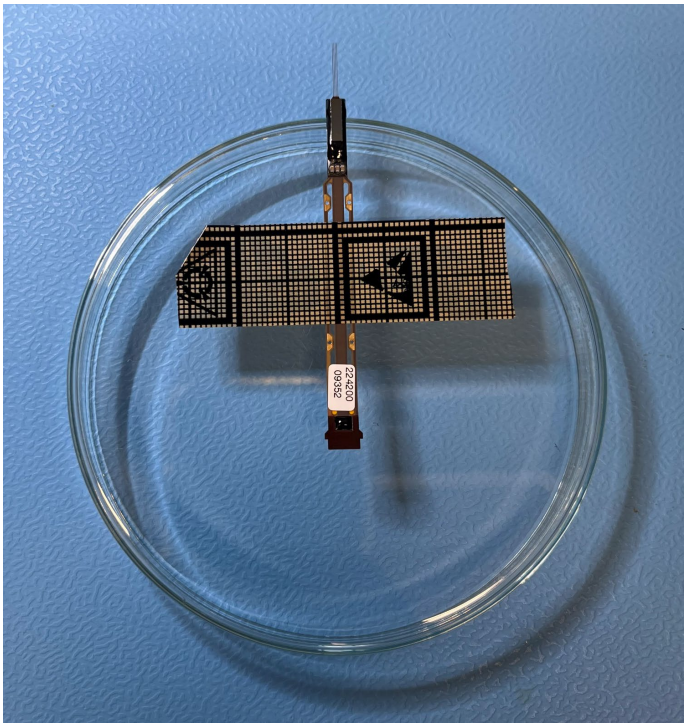


Figure 42: Fixing the probe before soldering.

- Clean the solder tip using a brass wire mesh or damp sponge. Repeat at frequent intervals.
- Wet the solder tip slightly with solder wire. This improves heat transfer from the iron to the solder pad.
- Insert the wire through the hole in the solder pad. Place the solder iron at the corner between the pad and the GND/REF wire. (Figure 43)

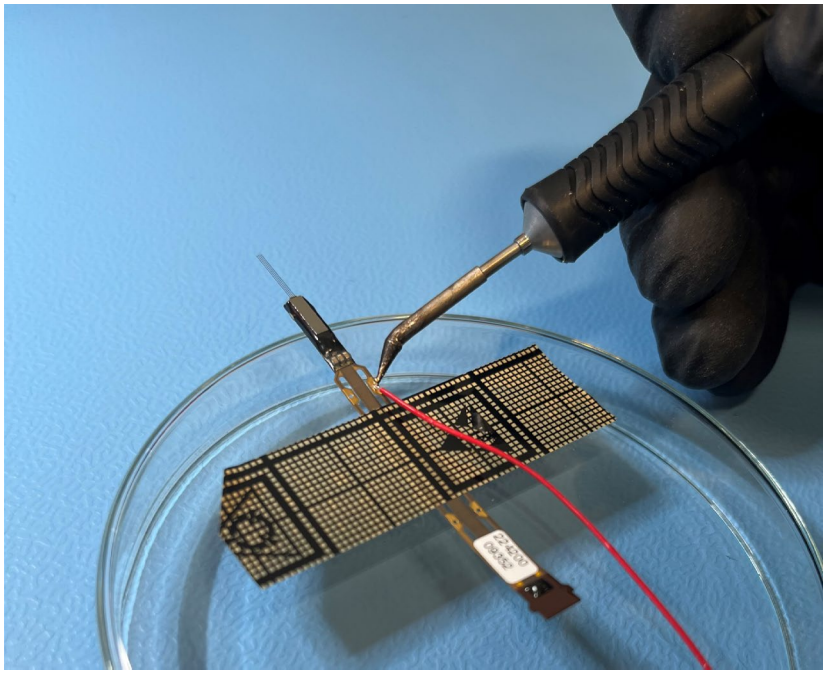


Figure 43: Placing the solder tip in the corner between wire and pad.

- Feed a small amount of solder to the corner between the solder tip and wire. The solder melts on the pad and the GND/REF wire. Solder wire can be purchased in different diameters. For this application it is advisable to use a smaller diameter (< 1 mm), also depending on the diameter of the GND/REF wire.
- The soldering time and temperature should be minimized to <4 s and max. 350°C, respectively.

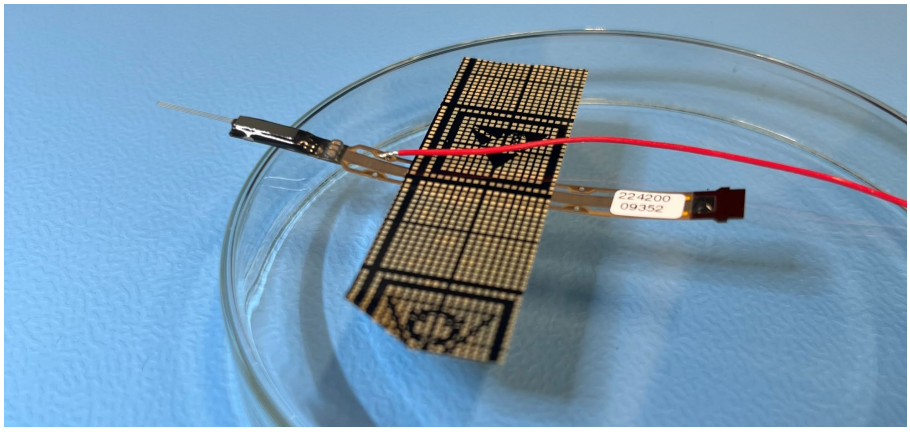


Figure 44: Wire soldered to the solder pad.

Always inspect the quality of the solder joint under a microscope before implanting. Also check the components surrounding the solder pads for eventual damage. Run the built-in self-tests after soldering to check the functionality of the probe.

IMPORTANT: Generally, poor connections are a common source of noise. The reference and ground connections on the probe and flex are critical as they are very close to the probe signal amplifiers. Please consult this website on best practices on soldering: Noise: Learn How To Solder - SpikeGLX (billkarsh.github.io).

Appendix C ESD Safety

To avoid ESD damage when handling the electronic hardware (probe, HS, PXIe, OneBox), the operator must be grounded via ESD protective equipment, such as a wrist wrap. General ESD guidelines can be found at: http://www.esda.org/about-esd/esd-fundamentals/part-3-basic-esd-control-procedures-and-materials/.

When the probe is implanted in an animal, special precautions are required; To protect the probe from ESD damage, potential static charge build-up on the animal must be discharged via a low-current path. ESD-compliant material must be used because the cables and connectors have an integrated 1M-10M resistor, which limits the current and thus induces a slow discharge rather than a spike.

Preventing static charge build-up on an animal can be challenging, especially when the animal is transported between locations (e.g., vivarium cage, transport cage, lab cage, operating table). Static charge build-up can be prevented by continuously keeping the animal on an ESD-compliant mat which is connected to earth ground via an ESD-compliant cable.

If continuous grounding of the animal is not feasible, the following guidelines should be followed:

- Grounding of the operator via ESD-compliant protective equipment when touching the animal.
- Grounding of the animal via ESD-compliant protective equipment prior to connecting the probe flex to the HS. This can be done, for example, by placing the animal on an ESD-compliant mat. Alternatively, if the external reference wire of the probe flex is connected to the animal's skull, the grounding can be done through this connection. This connection should be maintained throughout the experiment.
- Grounding of the probe flex ground pin or wire via ESD-compliant protective equipment prior to connecting the probe flex to the HS. This connection can be removed when the probe flex is plugged into the HS.
- Grounding of the PXIe module or OneBox to earth ground prior to connecting the probe flex to the HS. This is normally already achieved if the PXIe chassis or OneBox is plugged into the mains supply.

***NOTE**: A connection from the probe to the PXIe acquisition module ground does not provide an ESD-safe discharge path, because it does not contain a current-limiting resistor.*